worldskills

Standards and Assessment Guide

Electronics

V1.1

Introduction

Welcome to the Standards and Assessment Guide (SAG), a comprehensive resource designed to support excellence in assessment practices for all skills competitions hosted at the WorldSkills Competition. A key component of the SAG is the commitment to continuous improvement through ongoing review, ensuring that these guides consistently reflect the latest industry innovations and high standards of assessment in an open and transparent manner.

Purpose

The primary purpose of this guide is to provide a structured framework for the consistent and fair assessment of each skill competition. It aims to ensure that all assessments are conducted with a high degree of accuracy, reliability, validity, and reflect global industry standards. By adhering to these guidelines, assessors can maintain the integrity of the competition and uphold the high standards associated with WorldSkills.

Note: this guide is not a replacement for the Marking Scheme and should only be used as a reference when required during the assessment process. Competitors are not allowed to have a copy of this SAG in the workshop in either digital or paper form.

Scope

This document covers general assessment practices applicable to a diverse range of industry sectors including:

- Manufacturing and Engineering Technology
- Information and Communication Technology
- Construction and Building Technology
- Transportation and Logistics
- Social and Personal Services
- Creative Arts and Fashion

Each skill competition has its unique requirements and benchmarks, which are detailed within sections of this guide. The consistency of assessment across each skill is the overarching principle, ensuring a unified approach to evaluating Competitor performance to the highest standards.

Key Components

The guide is structured into several key components, each addressing critical aspects of the assessment process:

Assessment Principles and Objectives

- Emphasis on fairness, transparency, and objectivity in assessments.
- Alignment with global industry standards and best practices.

Assessment Methods and Tools

- Description of various assessment methods in Measurement and Judgement.
- Guidance on the application of appropriate assessment tools and equipment (if applicable).

Criteria and Benchmarks

- Examples of assessment criteria and aspects for each skill, outlining the expected competencies and performance standards.
- Benchmarks for different levels of proficiency i.e. Judgement award range 0, 1, 2, 3 or Yes/No criteria alongside clear measurable descriptors.

Expert assessment requirements

- Completion of the Access Programme.
- Approved Curriculum Vitae (CV).
- Reaching **100%** Expert preparedness.
- Full participation of online and in-person Mandatory Assessment Training (MAT).
- Completion of practical assessment testing at the Competition.

Quality Assurance and Improvement

- Monitoring and evaluation: Ensuring assessments are carried out correctly and produce reliable results.
- Continuous improvement: Using feedback from Experts and Skill Competition Managers to enhance future assessments.
- Periodic review: Regularly updating processes to reflect current industry and WorldSkills standards.

Implementation

For effective implementation, this guide should be used for guidance purposes only and in parallel with the Technical Description for each skill. Experts are encouraged to familiarize themselves thoroughly with both the general guidelines and the particular requirements of their respective skill areas. Collaborative efforts between the Skill Management Team, Experts, and Competitors are vital for achieving the ultimate goal of global skills development.

Conclusion

The Standards and Assessment Guide embodies the commitment of the WorldSkills movement to nurturing talent and promoting the highest standards of vocational education and training worldwide. By providing clear and comprehensive guidance, we aim to empower Experts to conduct marking and assessment practices that are not only rigorous and equitable but also inspiring and transformative for all participants.
Thank you for your dedication to upholding these standards and contributing to the success of the WorldSkills Competition. Together, we can continue to champion skills excellence and celebrate the achievements of talented individuals from around the globe

Skill 16 - Electronics

Measurement

- Measurement is used to assess accuracy, precision, and other performance that can be measured objectively. It is used where ambiguity must be avoided.
- The total marks allocated to measurement marking may vary from competition to competition depending on the Test Project.

Judgement

- Judgement is used to assess the quality of performance about which there may be small differences of view when applying the external benchmarks.
- The Resources column in the table below may include all kinds/formats of resources such as: a link to a YouTube video, a website link, an illustration, a photo, a reference to a book, and so on. It needs to be as detailed as possible to show the differentiation between 0, 1, 2, 3.

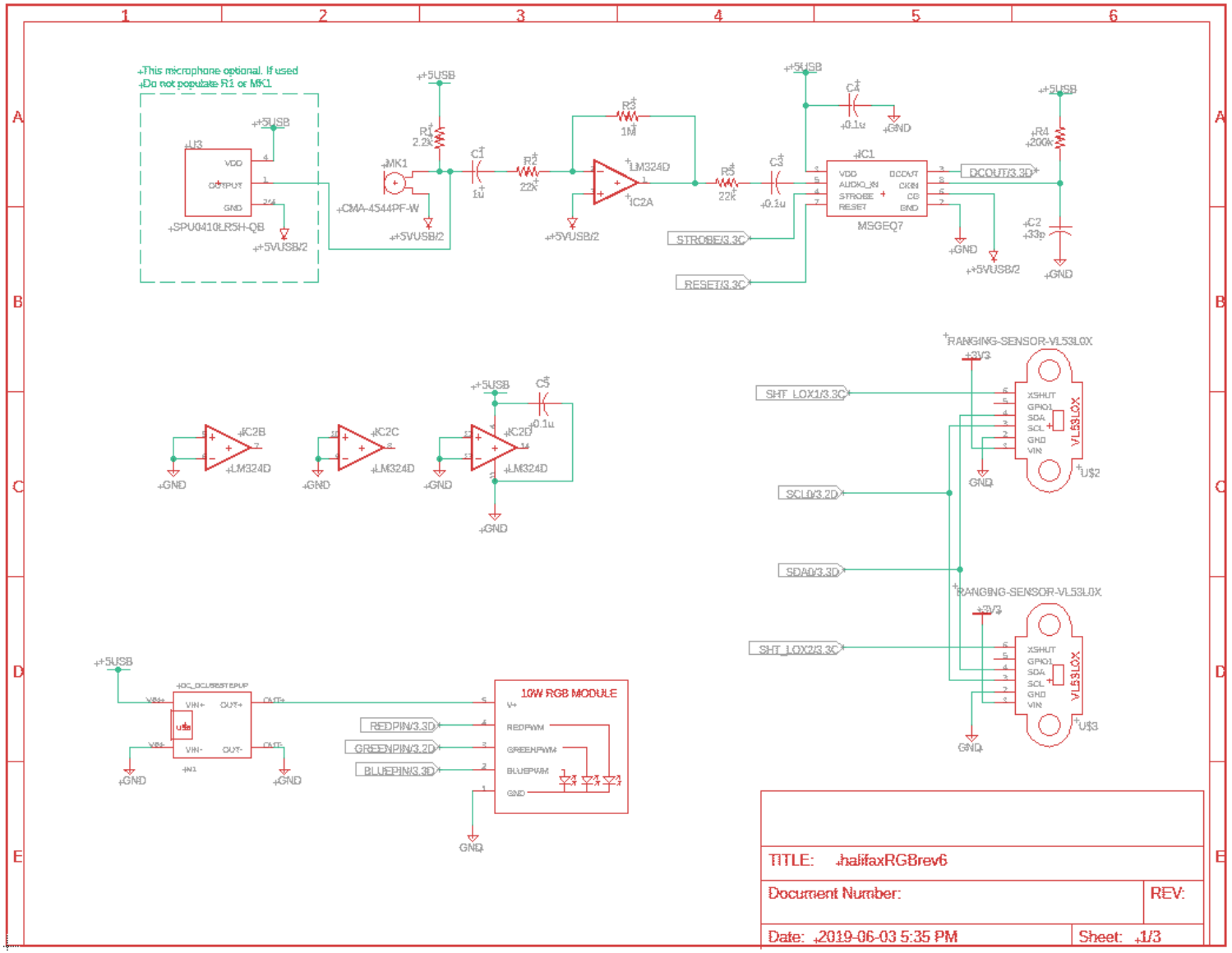
Generic judgement rules:

- The assessment group comprises three Experts plus one Expert who acts as the supervisor. The supervising Expert will replace an Expert in the marking group to prevent compatriot marking.
- The difference of the three Experts' scores may not exceed 1. If this is the situation the Experts must re-score until there is a maximum difference of 1. As long as the three Experts judge within 1, the result can be entered into the CIS.
- The total marks allocated to judgement marking may vary from competition to competition depending on the Test Project.

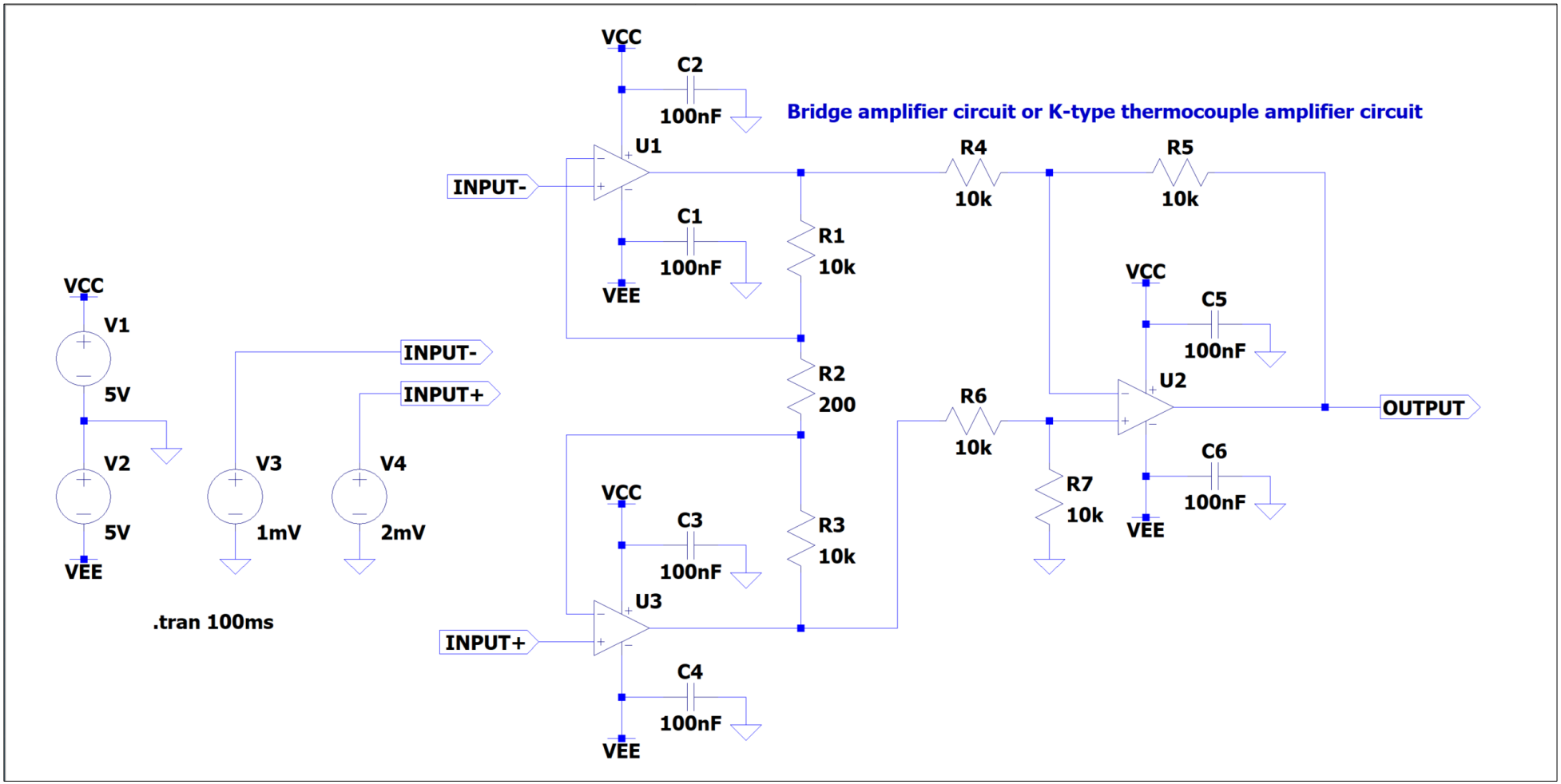
Circuit Design

Judgement Aspect: Circuit Design - Schematic Quality

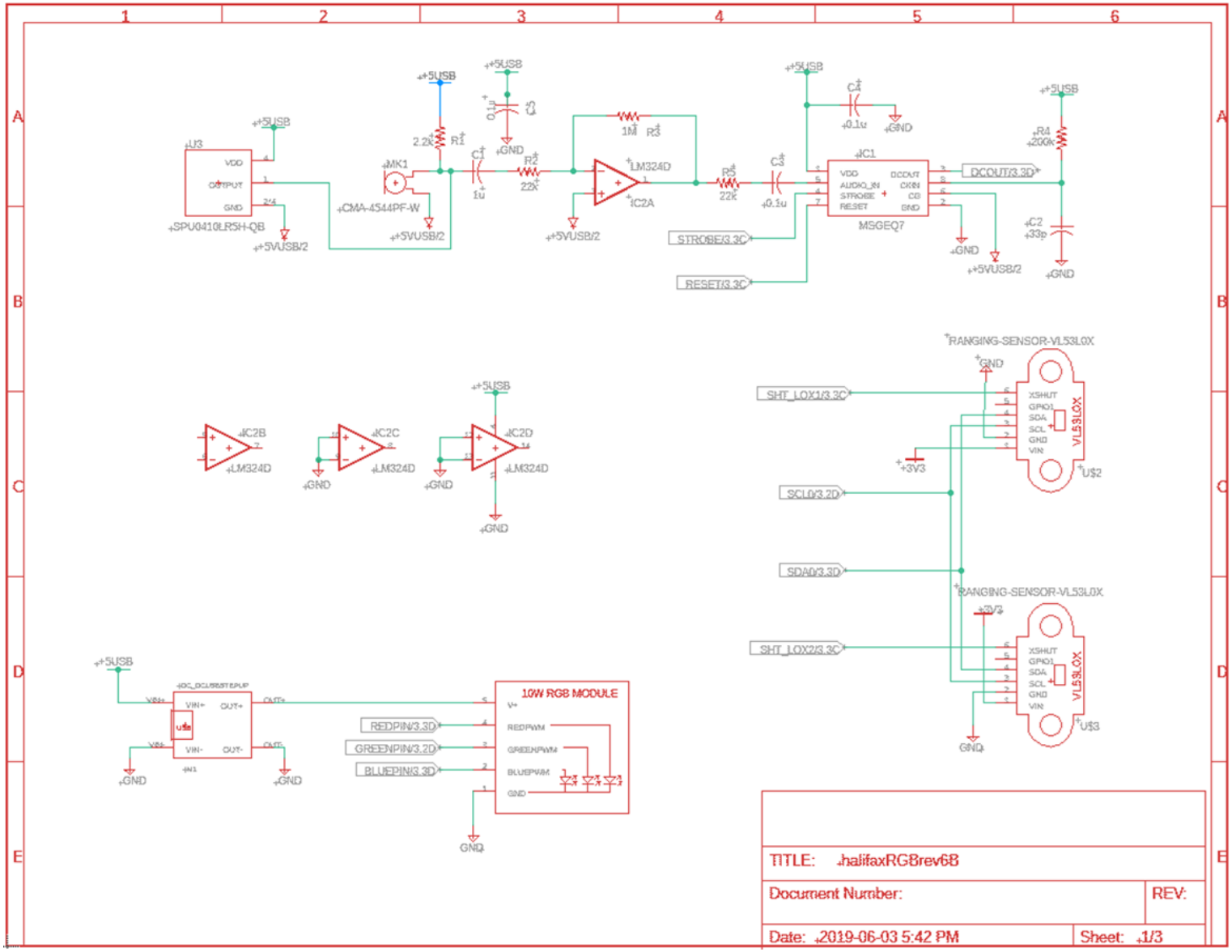
WSOS section as per TD	Points	Descriptor	Resource
2, 3	3	• Schematic is very easy to follow. • Signal flow from left to right (unless better clarity results from right to left signal flow). • Component number and designations always in the same plane and place. • +V at the top, GND and -V at the bottom. • Schematic is not crowded. • Supply rail connections to ICs grouped together and easily found. • Bypass Caps always placed beside IC they belong to, if they matter. Not needed for ideal voltage sources. E.g. needed for PSRR / CMRR / supply ripple simulations. • Unused inputs tied to GND (when necessary).	*See next page


This microphone optional. If used
Do not populate R1 or MK1
+5USB
U3
SPU0410LR5H-QB
+5VUSB/2
MK1
CMA-4544PF-W
R1
2.2k
C1
1u
R2
22k
R3
1M
LM324D
IC2A
R5
22k
C3
0.1u
C4
0.1u
IC1
MSGEQ7
STROBE/3.3C
RESET/3.3C
DCOUT/3.3D
R4
200k
C2
33p
IC2B
IC2C
IC2D
C5
RANGING-SENSOR-VL53L0X
+3V3
SHT_LOX1/3.3C
SCL0/3.2D
SDA0/3.3D
SHT_LOX2/3.3C
VL53L0X
U$2
U$3
10W RGB MODULE
REDPIN/3.3D
GREENPIN/3.2D
BLUEPIN/3.3D
REDPWM
GREENPWM
BLUEPWM
TITLE: halifaxRGBrev6
Document Number:
REV:
Date: 2019-06-03 5:35 PM
Sheet: 1/3

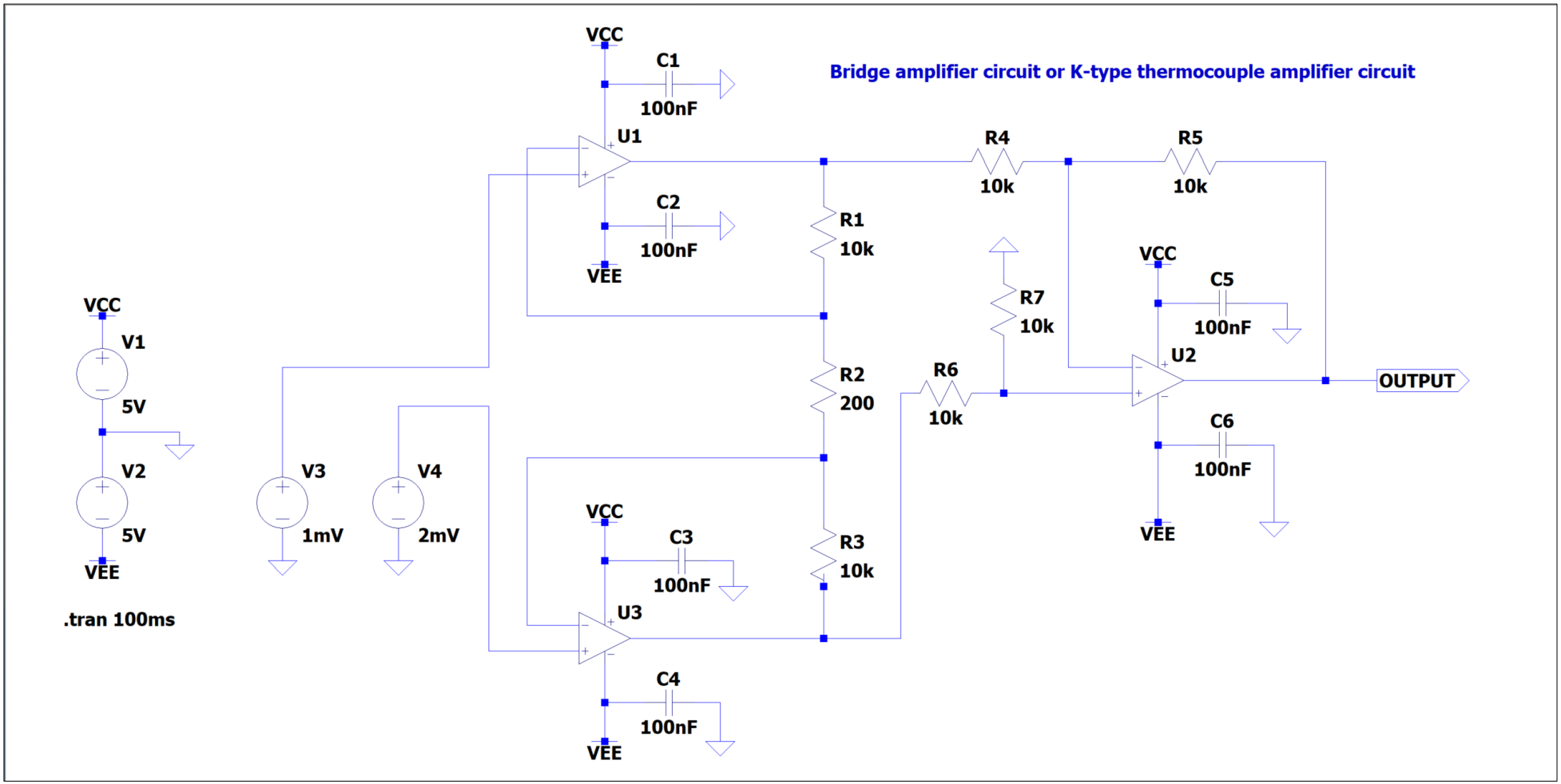
Case Based on LTspice



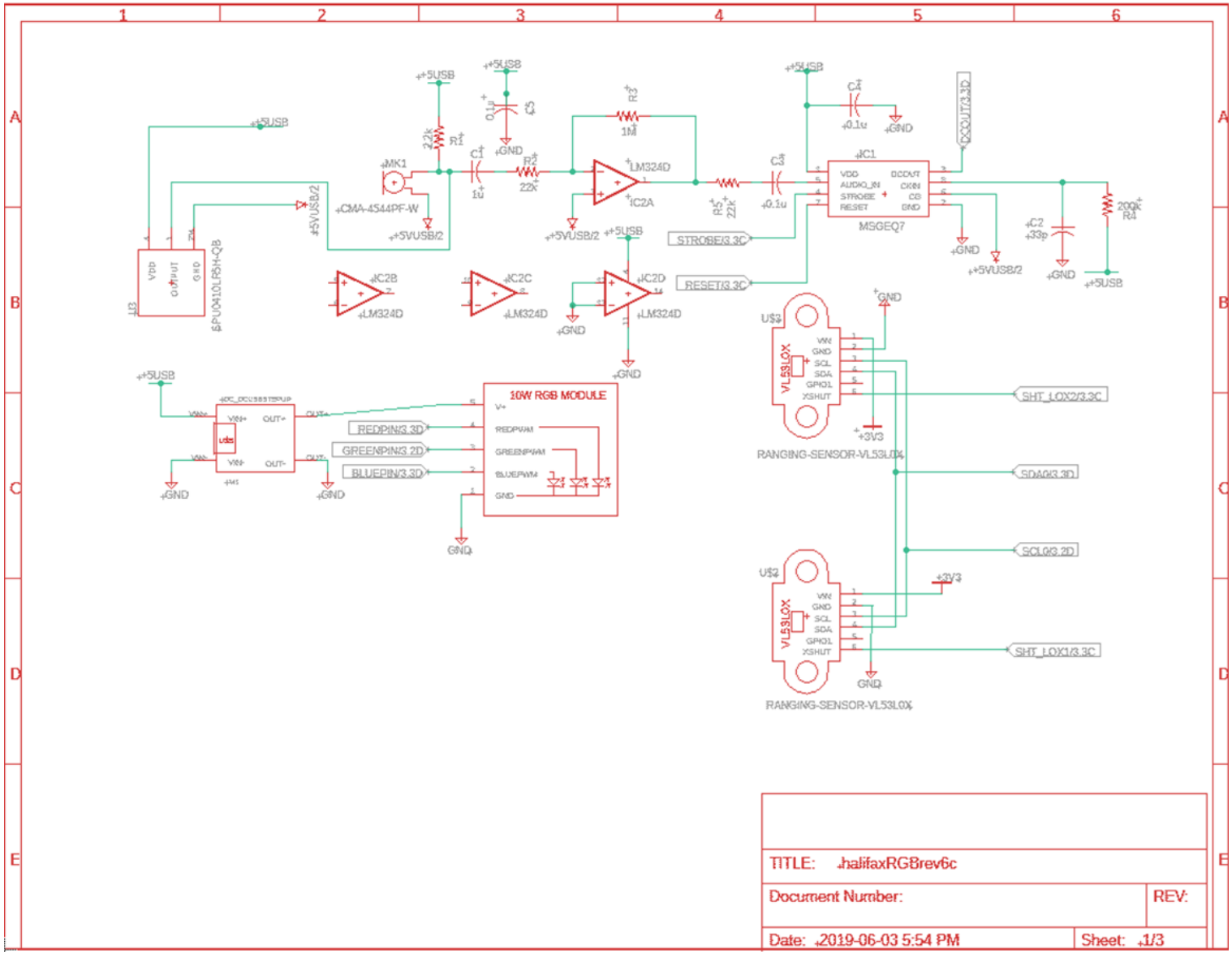
WSOS section as per TD	Points	Descriptor	Resource
2, 3	2	• Schematic is easy to follow. • Signal flow from left to right (unless better clarity results from right to left signal flow). • Component number and designations mostly in the same plane and place. • +V at the top, GND and -V at the bottom most of the time. • Schematic is not crowded. • Supply rail connections for ICs shown. • Bypass Caps mostly placed beside IC they belong to, if they matter. Not needed for ideal voltage sources. E.g. needed for PSRR / CMRR / supply ripple simulations. • Unused inputs mostly tied to GND.	*See next page


1
2
3
4
5
6
A
B
C
D
E
+5USB
+U3
VDD
OUTPUT
GND
+SPU0410LR5H-QB
+5VUSB/2
+MK1
+CMA-4544PF-W
2.2k R1
C1 1u
R2 22k
+LM324D
+IC2A
1M R3
R5 22k
C3 +0.1u
+IC1
VDD
AUDIO_IN
STROBE
RESET
DCOUT
CKIN
CB
GND
MSGEQ7
DCOUT/3.3D
STROBE/3.3C
RESET/3.3C
C4 +0.1u
R4 +20k
C2 +33p
+GND
+IC2B
+IC2C
+IC2D
+LM324D
+RANGING-SENSOR-VL53L0X
SHT_LOX1/3.3C
SCL0/3.2D
SDA0/3.3D
SHT_LOX2/3.3C
+3V3
XSHUT
GPIO1
SDA
SCL
GND
VIN
VL53L0X
+U$2
+U$3
10W RGB MODULE
REDPWM
GREENPWM
BLUEPWM
REDPIN/3.3D
GREENPIN/3.2D
BLUEPIN/3.3D
TITLE: halifaxRGBrev6B
Document Number:
REV:
Date: 2019-06-03 5:42 PM
Sheet: 1/3

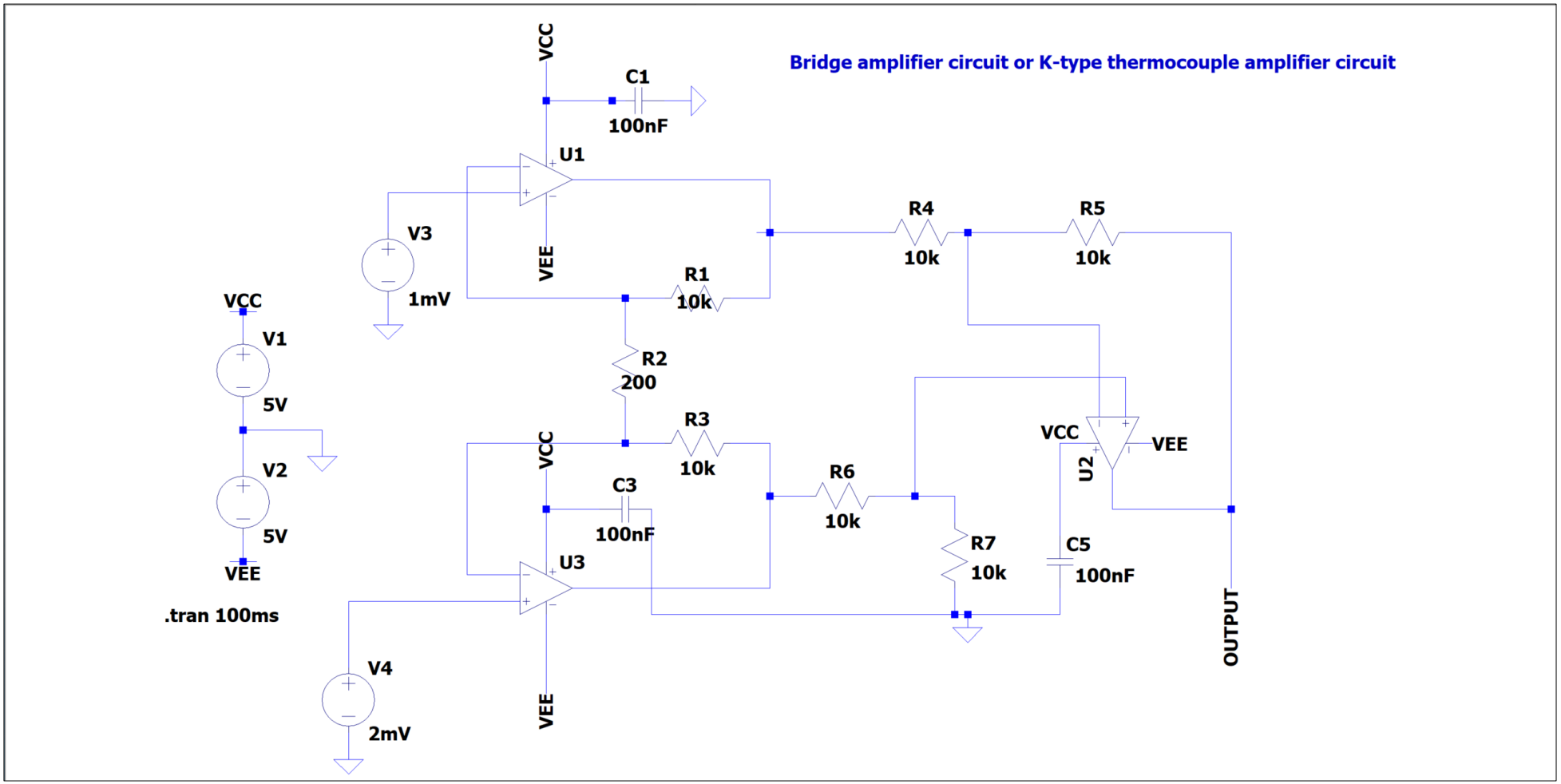
Case Based on LTspice



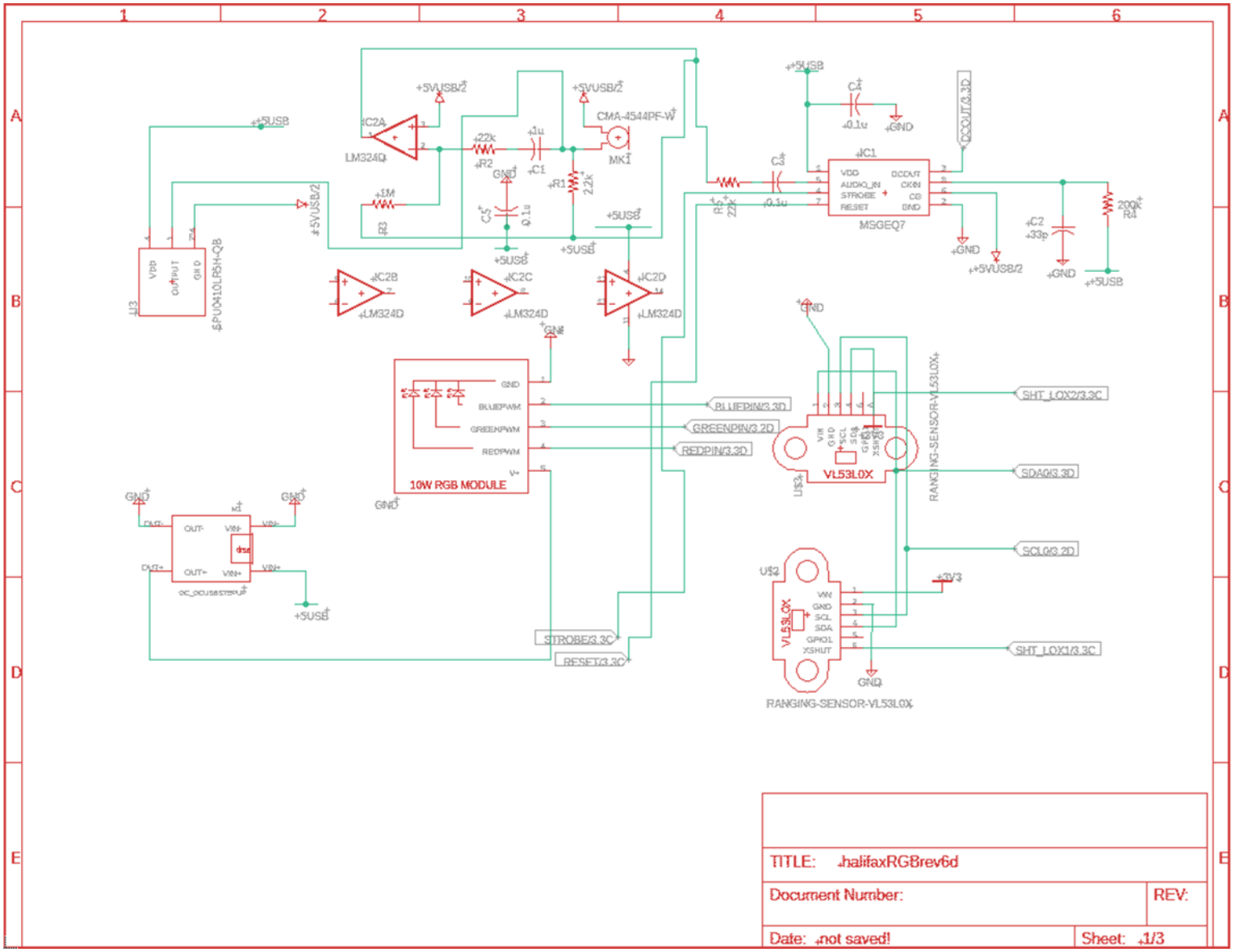
WSOS section as per TD	Points	Descriptor	Resource
2, 3	1	• Schematic is mostly correct. • Signal flow from left to right (unless better clarity results from right to left signal flow). • +V at the top, GND and -V at the bottom most of the time. • Schematic is crowded. • Supply rail connections for ICs shown. • Some long connecting wires used making the schematic hard to follow. • Bypass Caps present on schematic though often not near IC, if they matter. Not needed for ideal voltage sources. E.g. needed for PSRR / CMRR / supply ripple simulations. • Many unused inputs are not tied to GND.	*See next page


10W RGB MODULE
REDPIN/3.3D
GREENPIN/3.2D
BLUEPIN/3.3D
LM324D
MSGEQ7
STROBE/3.3C
RESET/3.3C
SHT_LOX2/3.3C
SDA0/3.3D
SCL0/3.2D
SHT_LOX1/3.3C
RANGING-SENSOR-VL53L0X
TITLE: .halifaxRGBrev6c
Document Number:
REV:
Date: .2019-06-03 5:54 PM
Sheet: .1/3

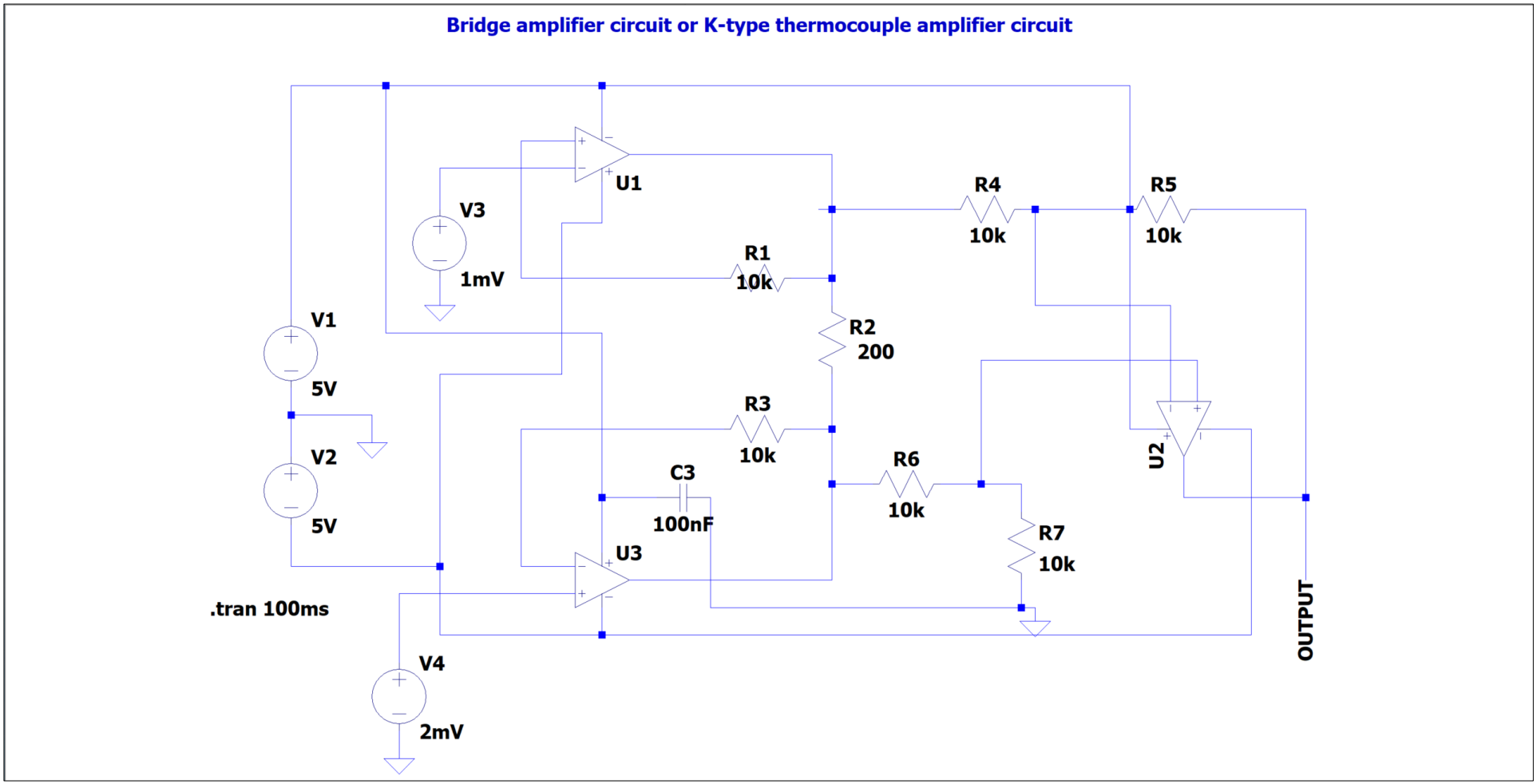
Case Based on LTspice



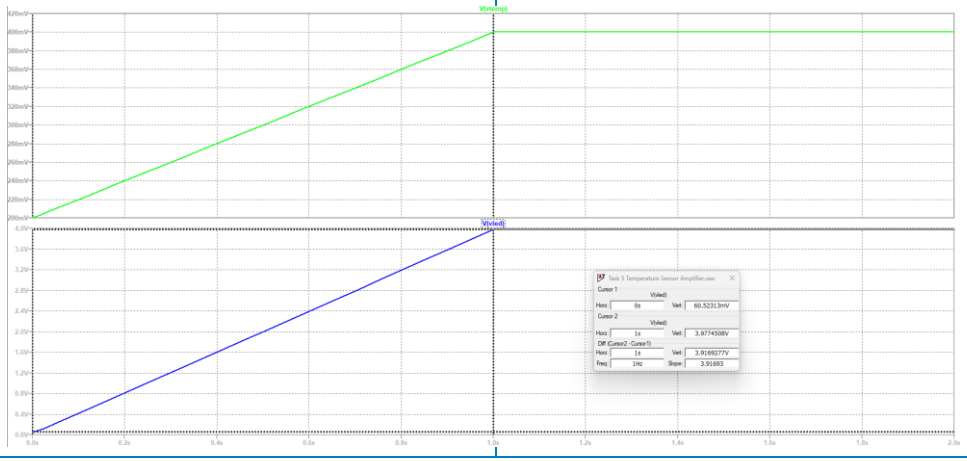
WSOS section as per TD	Points	Descriptor	Resource
2, 3	0	• The circuit is completely wrong and is not even close to the task requirements. • Schematic is incorrect. • No signal flow from left to right (unless better clarity results from right to left signal flow). • Component number and designations not used in many places. • +V at the bottom many times, GND and -V at the top many times. • Schematic is crowded. • Supply rail connections for ICs often missing. • Many long connecting wires used, making the schematic hard to follow. • Many bypass caps. missing, if they matter. Not needed for ideal voltage sources. E.g. needed for PSRR / CMRR / supply ripple simulations. • Unused inputs are not tied to GND at all.	*See next page

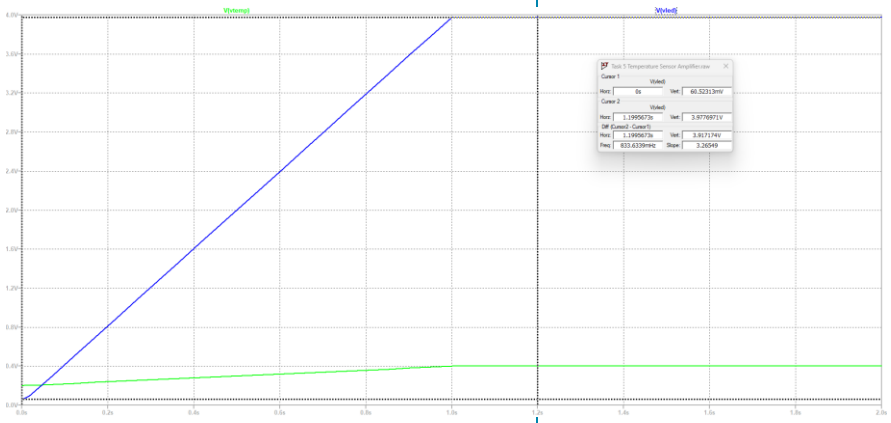

10W RGB MODULE
VL53L0X
MSGEQ7
LM324D
RANGING-SENSOR-VL53L0X
TITLE: halifaxRGBrev6d
Document Number:
REV:
Date: not saved!
Sheet: 1/3

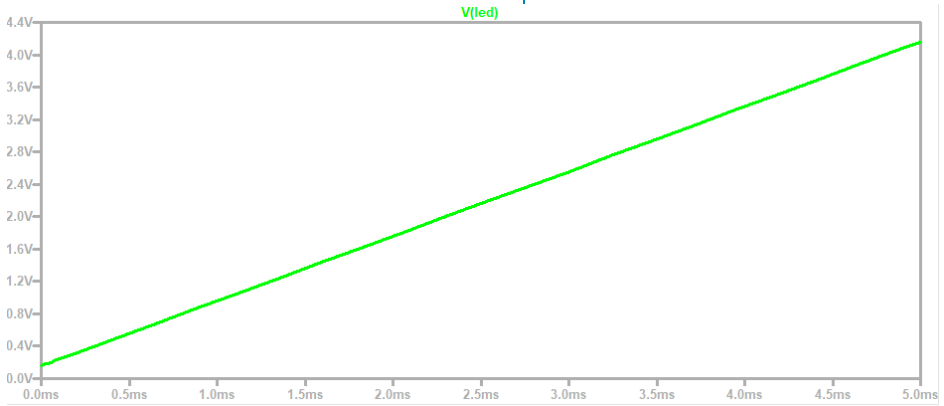
Case Based on LTspice



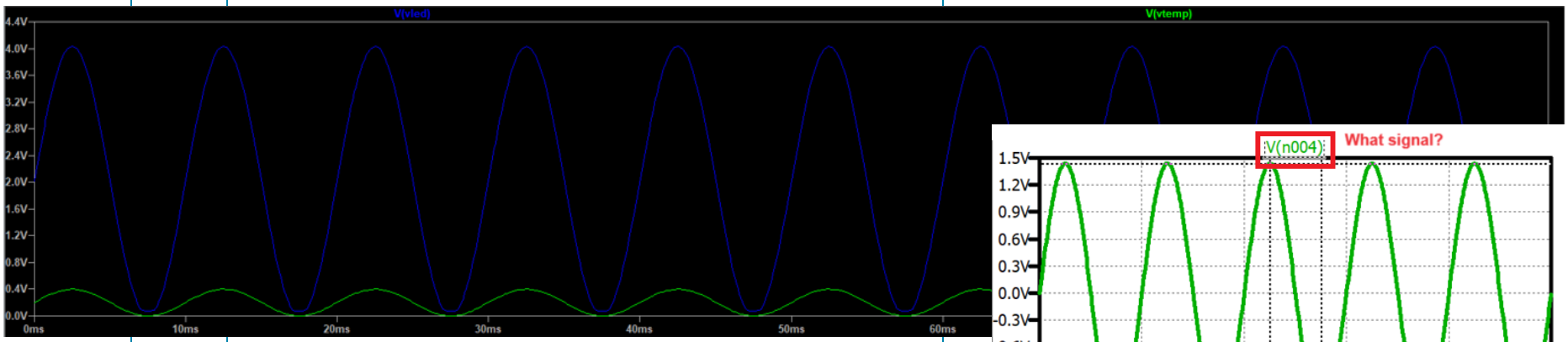
Judgement Aspect: Circuit Design - Simulation Quality

WSOS section as per TD	Points	Descriptor	Resource
2, 3	3	• A suitable simulation type (e.g. AC, DC, Transient, FFT, noise, etc.) is chosen. • The designed parameters (e.g. amplitude, frequency, duty cycle, cut-off frequency, etc.) are perfectly visible. • Scaling of the signals is done perfectly. • All relevant signals are shown and are labelled accordingly. • Cursors are used. • Good visibility. • The simulation is immediately understandable. It is perfectly clear, what the competitor wanted to simulate. 	**Example**: Temperature Sensor Amplifier This task involves receiving the signal VTEMP from the LM35, which will range from 200mV to 400mV (20°C to 40°C). It must convert this value to a signal ranging from 0V to 4V proportionally at the output, named VLED.

WSOS section as per TD	Points	Descriptor	Resource
2, 3	2	• A suitable simulation type (e.g. AC, DC, Transient, FFT, noise, etc.) is chosen. • The designed parameters (e.g. amplitude, frequency, duty cycle, cut-off frequency, etc.) are good visible. • Mostly all relevant signals are shown and are labelled accordingly. • Cursors are used but could be placed better. • Good visibility. • The simulation is mostly understandable. It is clear, what the competitor wanted to simulate. 	**Example**: Temperature Sensor Amplifier This task involves receiving the signal VTEMP from the LM35, which will range from 200mV to 400mV (20°C to 40°C). It must convert this value to a signal ranging from 0V to 4V proportionally at the output, named VLED.

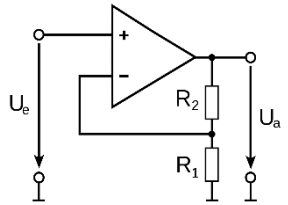
WSOS section as per TD	Points	Descriptor	Resource
2, 3	1	• A suitable simulation type (e.g. AC, DC, Transient, FFT, noise, etc.) is chosen. • The designed parameters (e.g. amplitude, frequency, duty cycle, cut-off frequency, etc.) are somehow visible. • Some relevant signals are shown and are labelled accordingly. • No Cursors are used. • Good visibility. • The simulation is difficult to understand. It is not directly clear, what the competitor wanted to simulate. 	**Example**: Temperature Sensor Amplifier This task involves receiving the signal VTEMP from the LM35, which will range from 200mV to 400mV (20°C to 40°C). It must convert this value to a signal ranging from 0V to 4V proportionally at the output, named VLED.

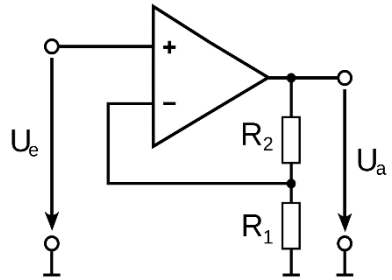
WSOS section as per TD	Points	Descriptor	Resource
2, 3	0	• The circuit is completely wrong and is not even close to the task requirements. • A not suitable simulation type is chosen. • The designed parameters (e.g. amplitude, frequency, duty cycle, cut-off frequency, etc.) are not visible at all. • No cursors are used when required • The simulation is not understandable. • Poor visibility • It is not clear which signal(s) is / are measured (e.g. labels are missing).	**Example**: Temperature Sensor Amplifier This task involves receiving the signal VTEMP from the LM35, which will range from 200mV to 400mV (20°C to 40°C). It must convert this value to a signal ranging from 0V to 4V proportionally at the output, named VLED.

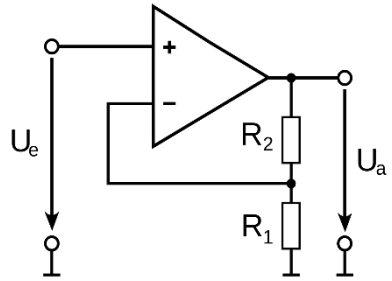


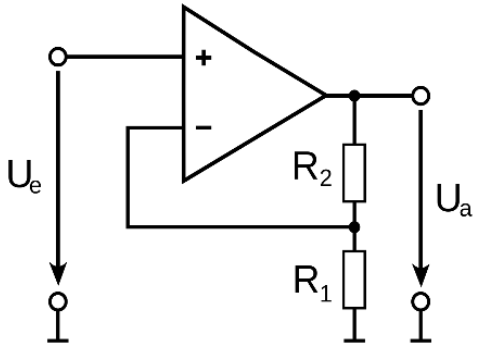
Judgement Aspect: Circuit Design - Calculation Quality

Optional, only if specifically required in instructions!

WSOS section as per TD	Points	Descriptor	Resource
2, 3	3	• The calculations have been made properly and are understandable. • The calculations are readable. • Make visible which components are given or selected. • Correct formula according to the circuit is used. • The subscripts of the formula and the circuit correspond. • All values are used with their corresponding units. • Correct prefixes (e.g. R, C, L, U, V, I) are used. • The final calculated value is rounded to an E-series number from the BOM. • **Specified values (e.g. gain, voltage, frequency, etc.) must be re-calculated with NSV / BOM values. → Approve, that the result is within the tolerance.**	**Example**: Non-Inverting Amplifier  given value(s): A = 5 (+- 5%) -) chosen value(s): R1 = 1kΩ -) formula for used circuit: $A = \frac{U_a}{U_e} = 1 + \frac{R_2}{R_1}$ R2 = R1 ∗ (A − 1) = 1KΩ ∗ (5 − 1) = 4KΩ -) choose E-Series / BOM: R2 = 3.9KΩ **-) <u>Approve Gain A tolerance:</u>** A = 5 (±5%) = 4. 75 … 5. 25 $\boldsymbol{A = \frac{U_a}{U_e} = 1 + \frac{R_2}{R_1} = 1 + \frac{3.9\text{k}\Omega}{1\text{k}\Omega} = 4.9}$ ✓

WSOS section as per TD	Points	Descriptor	Resource
2, 3	2	• The calculations have been made properly and are understandable. • The calculations are readable (important for handwritten calculations). • Make somehow visible which components are given or selected. • Correct formula according to the circuit is used. • The subscripts of the formula and the circuit mostly correspond. • All values are used with their corresponding units. • Mostly correct prefixes (e.g. R, C, L, U, V, I) are used. • The final calculated value is rounded to an E-series number from the BOM. • Approval of tolerance with NSV / BOM values is missing.	**Example**: Non-Inverting Amplifier  -) A = 5 -) R_1 = 1kΩ -) formula for used circuit: $A = \frac{U_a}{U_e} = 1 + \frac{R_2}{R_1}$ $R_2 = R_1 * (A - 1) = 4k\Omega$ -) choose E-Series / BOM: $R_2 = 3.9k\Omega$

WSOS section as per TD	Points	Descriptor	Resource
2, 3	1	• The calculations are readable (important for handwritten calculations). • Make somehow visible which components are given or selected. • Correct formula according to the circuit is used. • The subscripts of the formula and the circuit mostly correspond. • Some values are used with no or wrong units. • Some prefixes (e.g. R, C, L, U, V, I) are wrong. • The final calculated value is not rounded to an E-series number from the BOM. • Approval of tolerance with NSV / BOM values is missing.	**Example**: Non-Inverting Amplifier  -) A = 5 -) R_2 = 1k -) formula for used circuit: $A = \frac{U_a}{U_e} = 1 + \frac{R_2}{R_1}$ $R_2 = R_1 * (A - 1) = 4k\Omega$

WSOS section as per TD	Points	Descriptor	Resource
2, 3	0	• The circuit is completely wrong and is not even close to the task requirements. • The calculations are not readable and understandable at all. • Not visible which components are given or selected. • Wrong formula is used. • The subscripts of the formula and the circuit mostly correspond. • Some values are used with no or wrong units. • Some prefixes (e.g. R, C, L, U, V, I) are wrong. • The final calculated value is not rounded to an E-series number from the BOM. • Approval of tolerance with NSV / BOM values is missing.	**Example**: Non-Inverting Amplifier  -) Formula for used circuit: $A = \frac{U_a}{U_e} = -\frac{R_1}{R_2}$

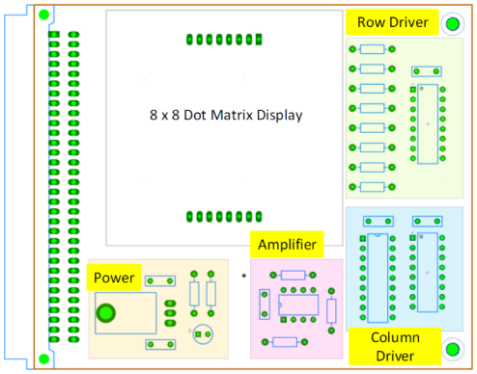
Example Measurement Aspects: Circuit Design

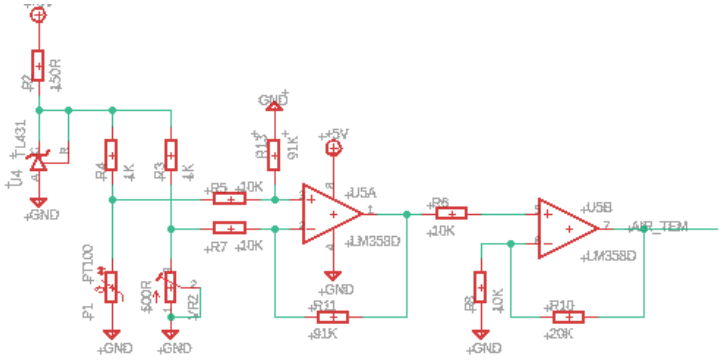
Aspect	WSOS section as per TD	Descriptor
Circuit Design	3	Circuit Design is working according to the task requirements. The circuit's efficiency (power, costs, etc.) does not matter if not specifically requested
Circuit Design	3	Circuit Design only uses components from BOM and NSV. BOM: Bill of Material, NSV:... Nominal Standard Value (e.g. E24-series)
Circuit Design	3	Calculation of value(s) is / are correct.

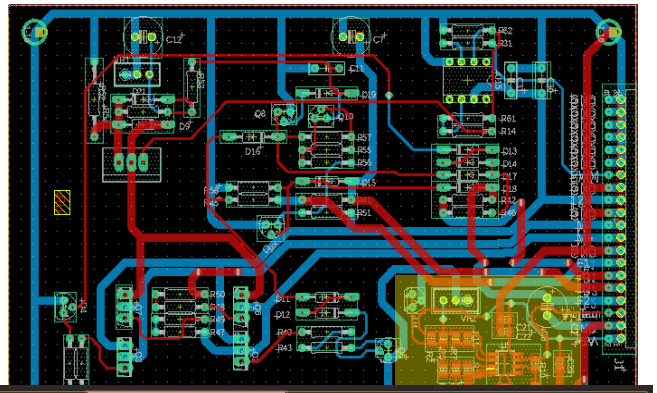
PCB Design

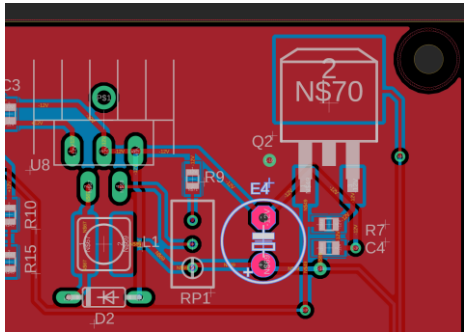
Judgement Aspect: PCB Design - Component Grouping and Placement

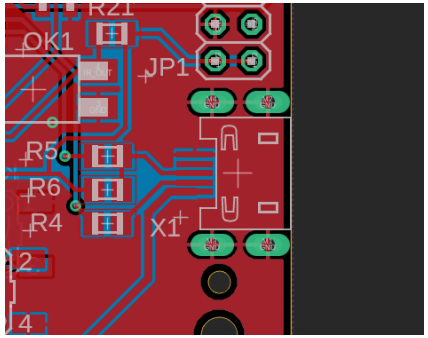
WSOS section as per TD	Points	Descriptor	Resource
3	3	• Components are grouped together by function. • There are subgroups of analog circuits, digital circuits, power supply circuits etc. • Grouping minimizes trace length between components and functional blocks. • All the temperature sensitive devices (like Electrolytic caps, temperature sensors) are separated from heat producing components. • All components have no mechanical interference or no mechanical interference in the operation area. • The orientation of the Bluetooth or Wi-Fi model antenna is facing outside the board, and there is no routing below the antenna.	Highlighted area shows the area(s) used by components by one group on schematic shown below. See next page.

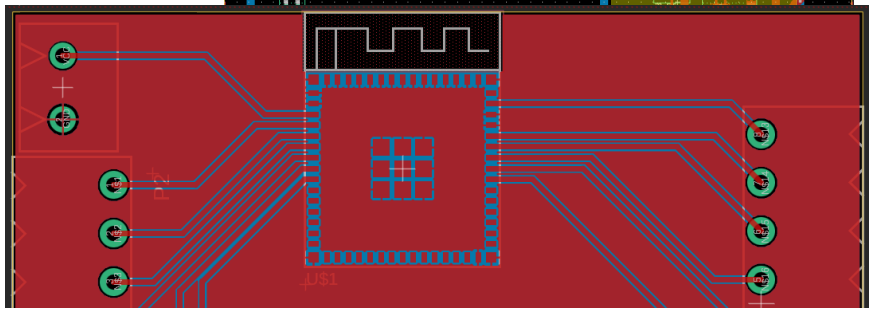

Row Driver
8 x 8 Dot Matrix Display
Amplifier
Power
Column
Driver


LM358D
LM358D

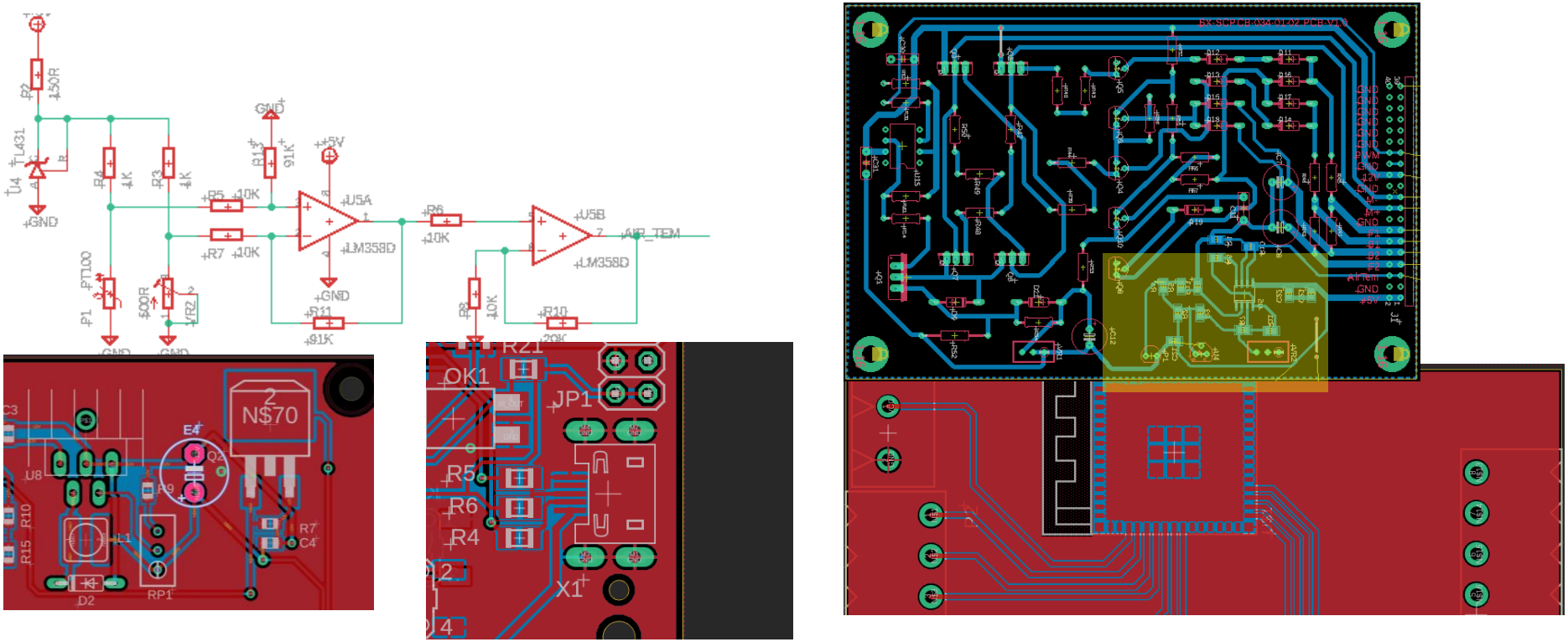



N$70
Q2
U8
R9
R10
R15
L1
RP1
D2
R7
C4

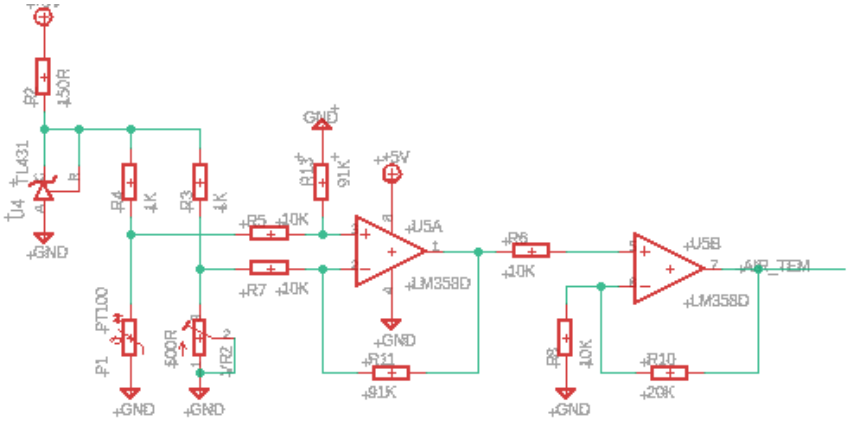

JP1
R5
R6
R4
X1

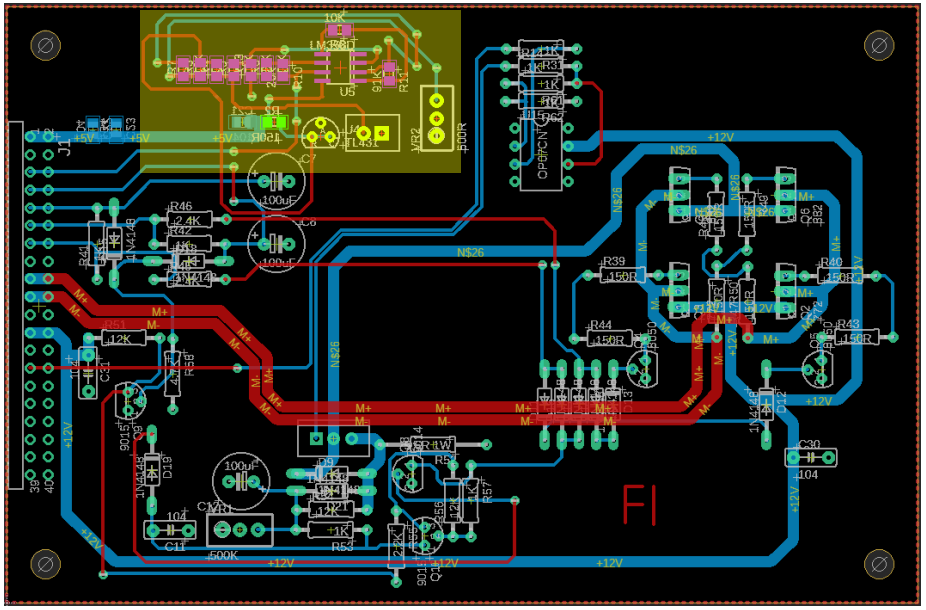


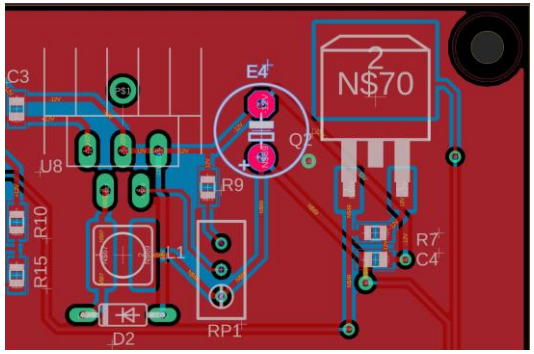
WSOS section as per TD	Points	Descriptor	Resource
3	2	• Most components grouped by function and optimally placed. • There are rare cases of some un-subgrouping of analog circuits, digital circuits, power supply circuits and etc. • Some noticeable variation in layout density. • Some temperature sensitive devices are located near to the heat producing components • Some components positions are not optimal, posing a risk of mechanical interference in the operating area. • The orientation of the Bluetooth or WiFi model antenna is Not facing outside the board, and there is no routing below the antenna.	Highlighted area shows the area(s) used by components by one group on schematic shown on the left. See next page.

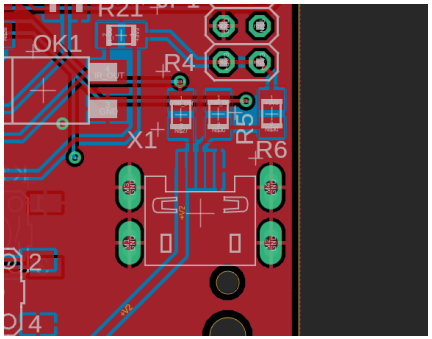

TL431
LM358D
LM358D
N$70
OK1
JP1
R5
R6
R4
X1

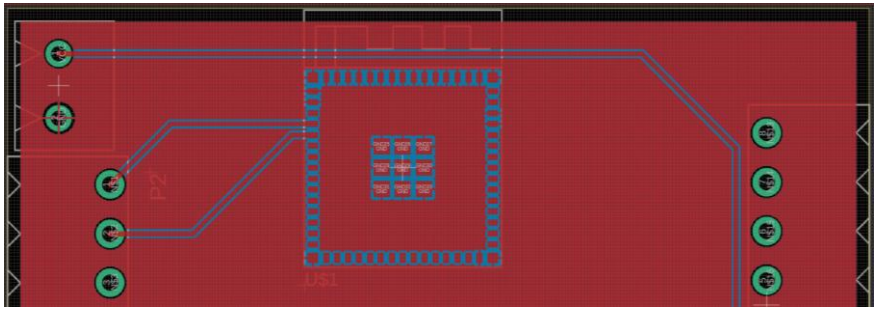
WSOS section as per TD	Points	Descriptor	Resource
3	1	• Some grouping by functional block. • Some subgroupings of analog circuits, digital circuits, power supply circuits and etc. • Some components not placed to optimize conductor length. • Wide variation in component layout density. • Some temperature sensitive devices are located closer to the heat producing components • Some components are placed or oriented incorrectly, which may cause interference in the operating area. • The orientation of the Bluetooth or WiFi model antenna is facing outside the board, but there is routing below the antenna.	Highlighted area shows the area(s) used by components by one group on schematic shown on the left. See next page.


U4 TL431
R2 150R
R4 1K
R3 1K
R5 10K
R7 10K
R14 91K
U5A
LM358D
R6 10K
U5B
LM358D
R8 10K
R10 20K
P1 PT100
500R
VR2
+5V
+GND
+91K

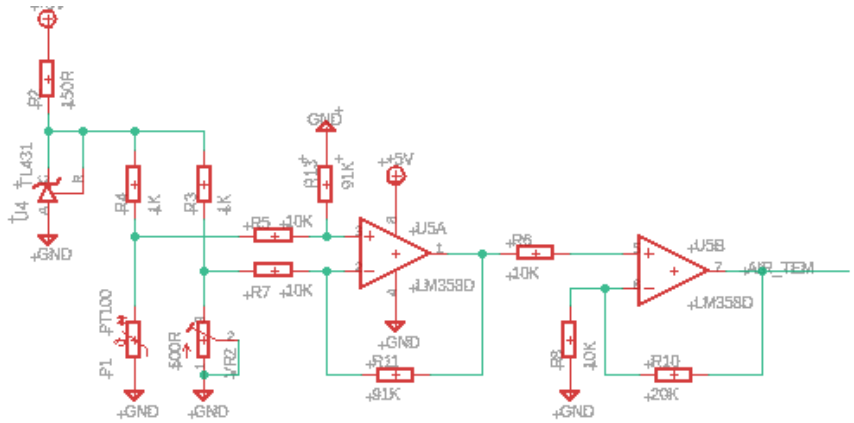

U5
LM358D
OP07CN
VR2
500R
R46 2.4K
R39 150R
R40 150R
R44 150R
R43 150R
C30 104
100uF
500K
FI
+12V

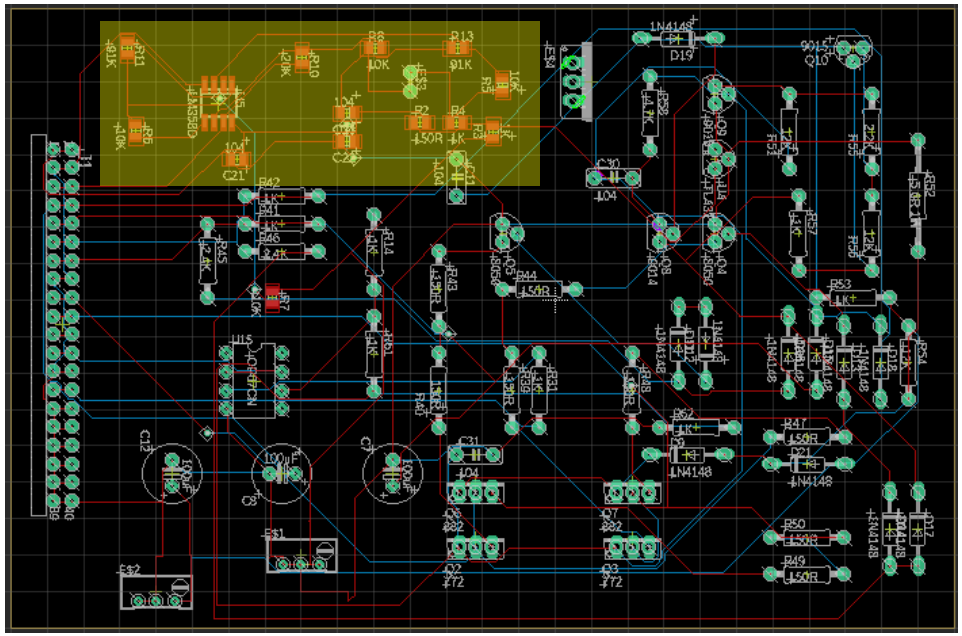

C3
E4
N$70
Q2
U8
R9
R10
R15
L1
R7
C4
D2
RP1

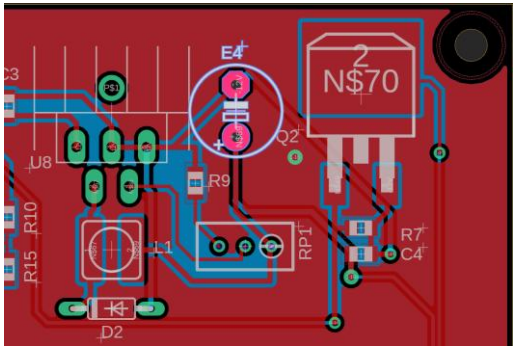

OK1
R4
R5
R6
X1

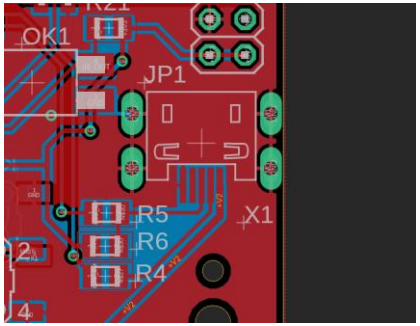

U$1

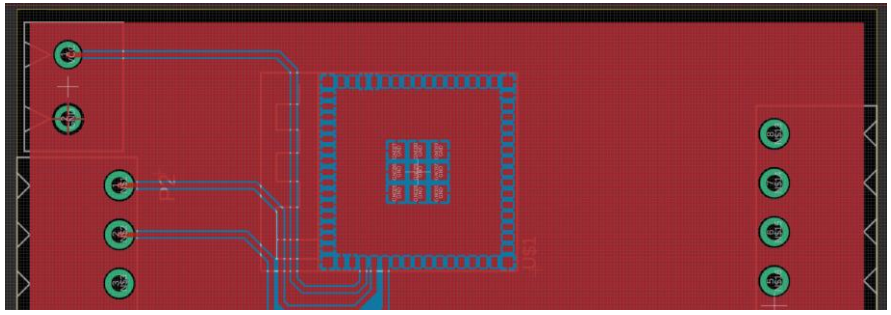
WSOS section as per TD	Points	Descriptor	Resource
3	0	• No noticeable grouping or • Pre-defined component positions are wrong. • Some temperature sensitive components have come into contact with the heating device. • Some components are placed or oriented incorrectly, resulting in obvious mechanical interference in the operating area. • The orientation of the Bluetooth or WiFi model antenna is Not facing outside the board, and there is routing below the antenna.	Highlighted area shows the area(s) used by components by one group on schematic shown on the left. See next page


TL431
+GND
+5V
+U5A
+U5B
+LM358D
+10K
+91K
+20K
+AN0_TEM

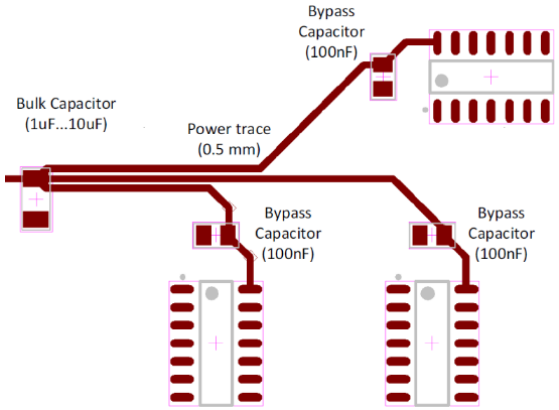
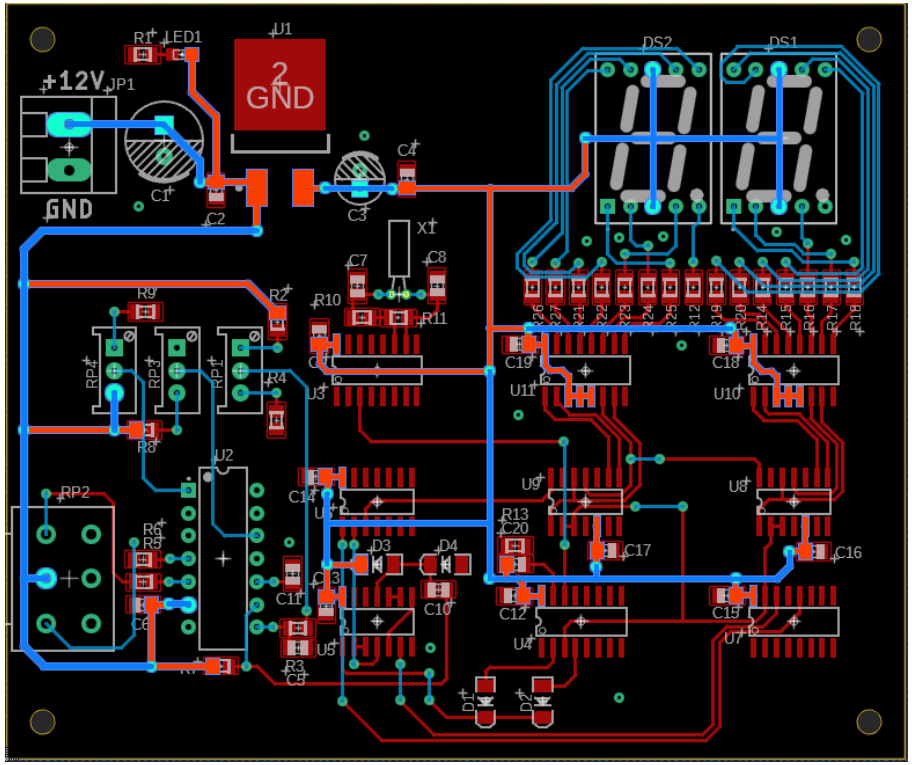


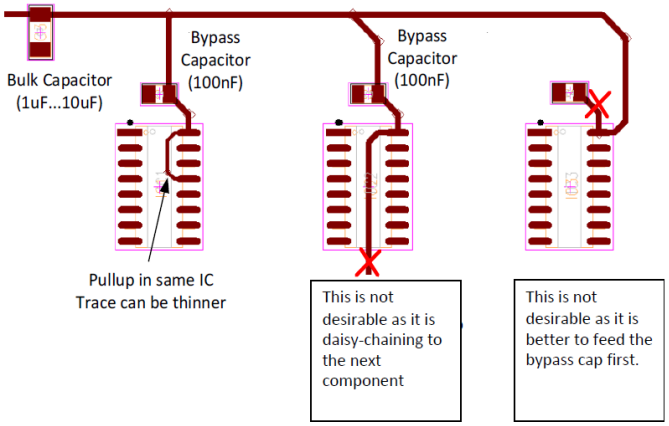
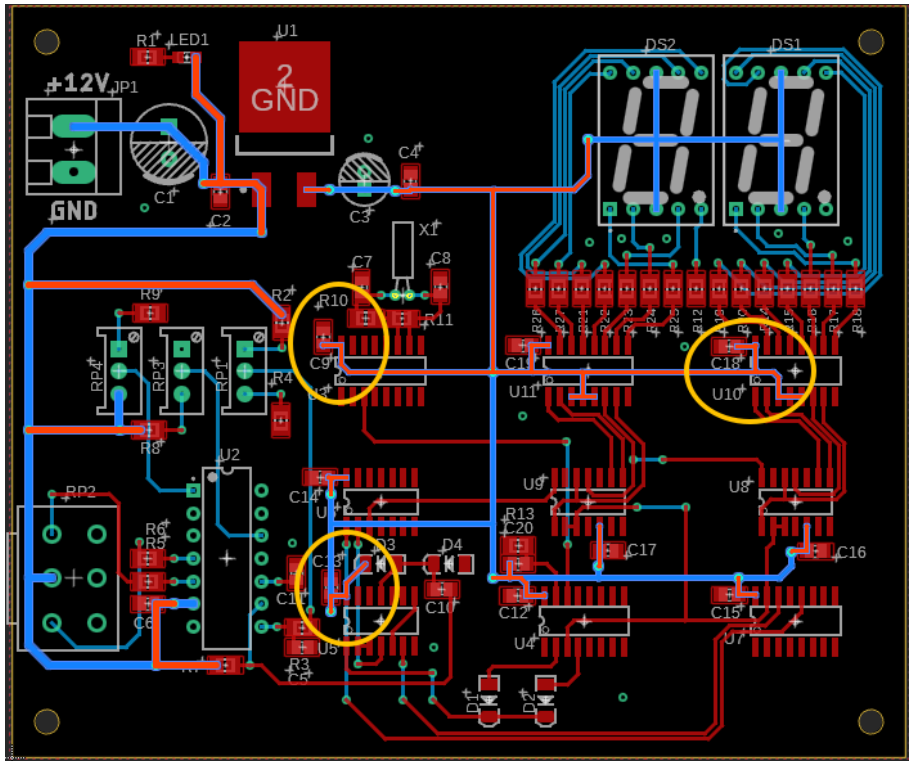

E4
N$70
Q2
U8
R9
R10
R15
L1
RP1
R7
C4
D2

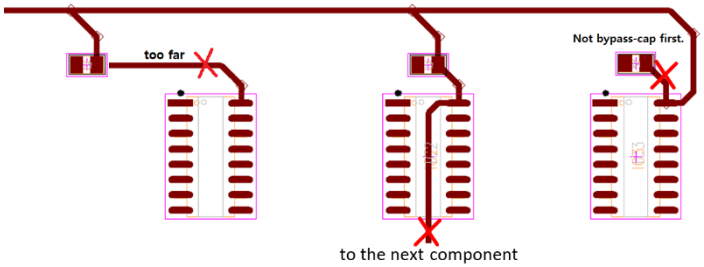
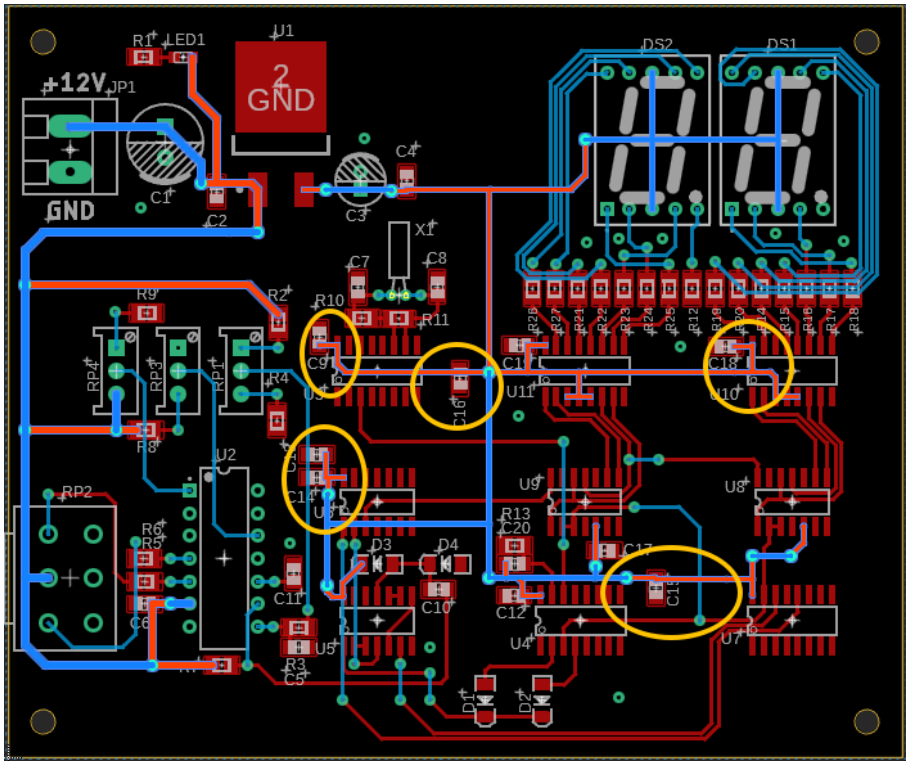

OK1
JP1
R5
R6
R4
X1

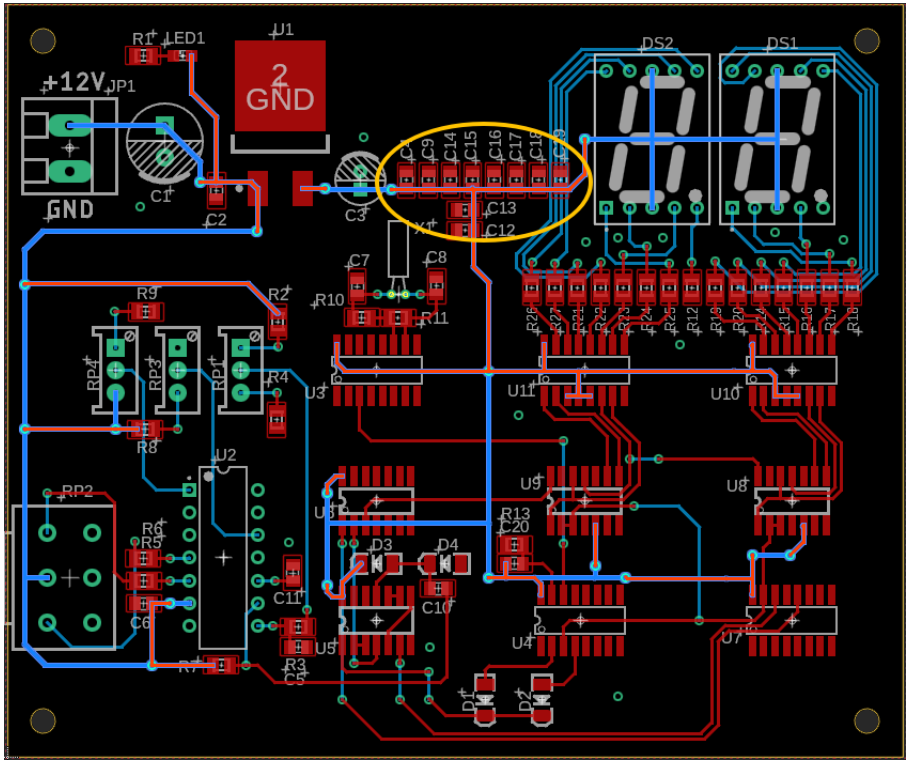


Judgement Aspect: PCB Design - Power Supply Routing and Bypass Capacitors

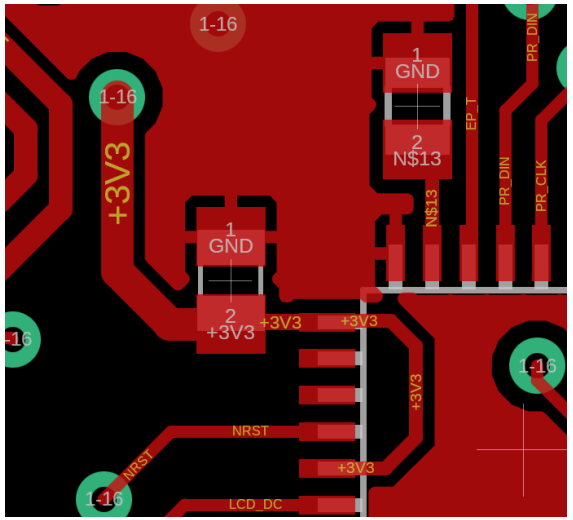
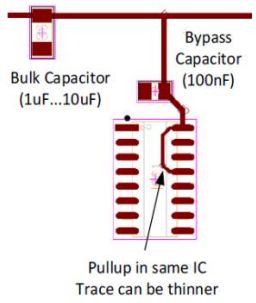
WSOS section as per TD	Points	Descriptor	Resource
3	3	• Bypass caps. are placed in the right place (near IC, VDD pin, etc.). • Routing is "star" style from connection of power supply components for main blocks of power loading (CPU, interfaces, display, RAM/ROM, Bluetooth, WiFi and etc.) • Routing is "star" style from connection of high power devices or devices sensitive to power fluctuations (high-precision operational amplifiers, small signal output sensors, PWM motor controllers, voltage reference sources, etc.) • No cascading of ICs supply rails. 	

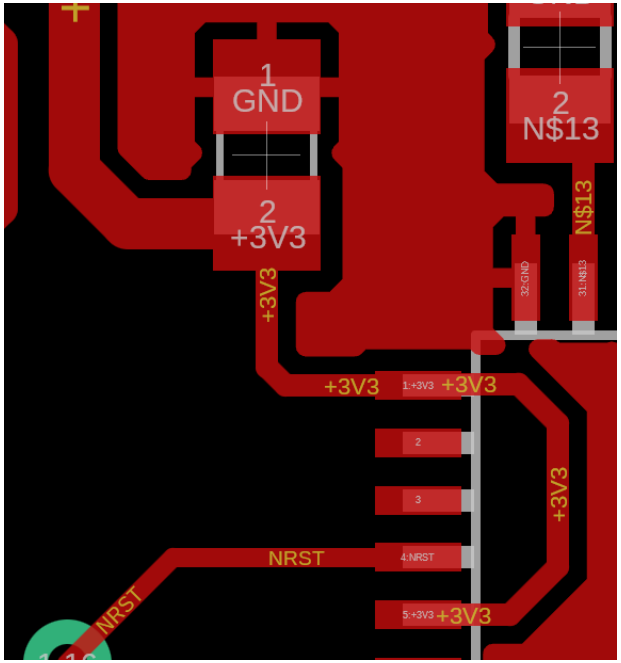
WSOS section as per TD	Points	Descriptor	Resource
3	2	• Some bypass-caps are placed too far from power pin. • Some routings are daisy-chaining to the next component. • Some routings are not “star” style for load blocks. 	

WSOS section as per TD	Points	Descriptor	Resource
3	1	• Many bypass-caps are placed too far from power pin. • Many routings are daisy-chaining to the next component. • Only a few blocks are “star” style routed. 	

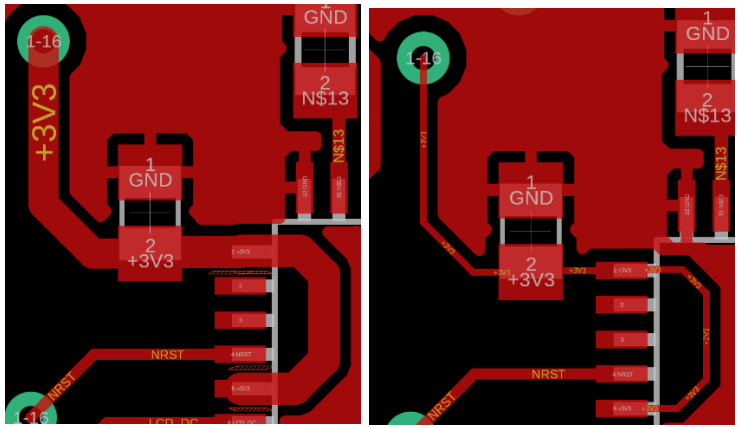
WSOS section as per TD	Points	Descriptor	Resource
3	0	• No bypass caps. used at all. • Too many routings are daisy-chaining to the next component. • Most of the widths of the power traces do not meet the requirements. • No “star” style routing. • Not all power supply traces are routed.	

Judgement Aspect: PCB Design - Power Supply Trace Width

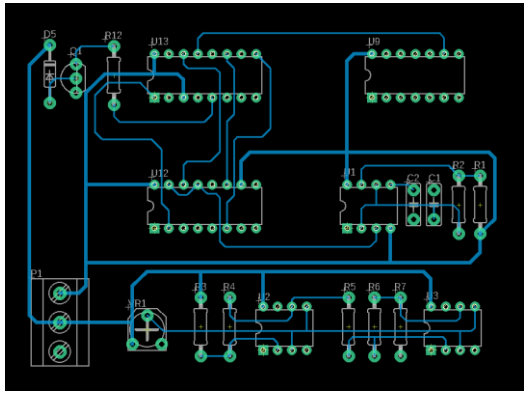
WSOS section as per TD	Points	Descriptor	Resource
3	3	• All Power supply traces are at a minimum able to handle the current through them according to IPC-2152 and are according to the width specification / design rules of the task description. • 10 mils (0.25 mm) 0.3 Amps • 16 mils (0.4mm) 0.4 Amps • 20 mils (0.5mm) 0.7 Amps • 24 mils (0.6mm) 1.0 Amps • 50 mils (1.3 mm) 2.0 Amps • 100 mils (2.5mm) 4.0 Amps • 150mils (4 mm) 6.0 Amps • Connections between bypass caps and component pins have a smaller width if pad is smaller than the minimum power trace width. The length of the segment with reduced width is kept at a minimum length • Connections on power supply nets that don't carry a significant current, can be smaller (e.g. pullup/pulldown)	 

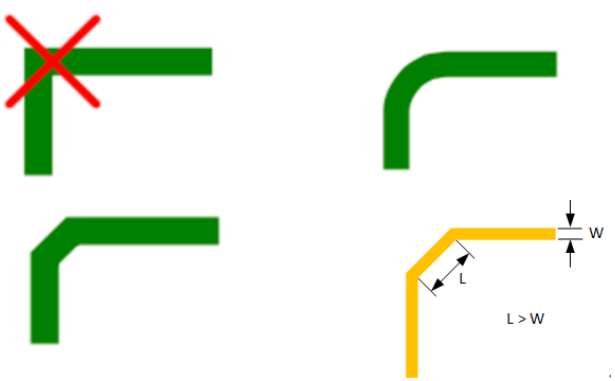
WSOS section as per TD	Points	Descriptor	Resource
3	2	• All Power supply traces are at a minimum able to handle the current through them according to IPC-2152 and are according to the width specification / design rules of the task description. • Connections between bypass caps and component pins have a smaller width if pad is smaller than the minimum power trace width. The length of the segment could be shorter • Connections on power supply nets that don't carry a significant current, can be smaller (e.g. pullup/pulldown)	

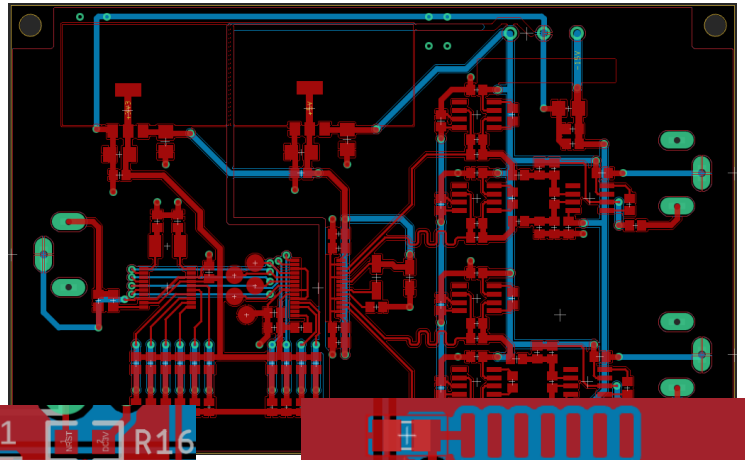
WSOS section as per TD	Points	Descriptor	Resource
3	1	• Most Power supply traces are at a minimum able to handle the current through them according to IPC-2152 and are according to the width specification / design rules of the task description.	

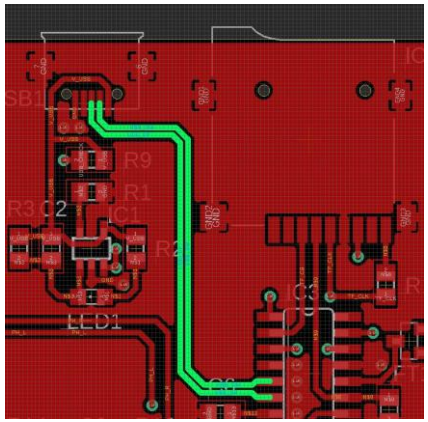
WSOS section as per TD	Points	Descriptor	Resource
3	0	• Power supply traces do not meet requirements at all • Critical design rule violations	

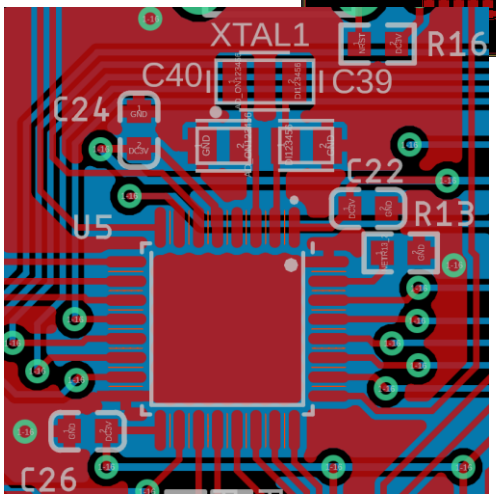
Judgement Aspect: PCB Design - Routing For Everything Other Than Power Supply

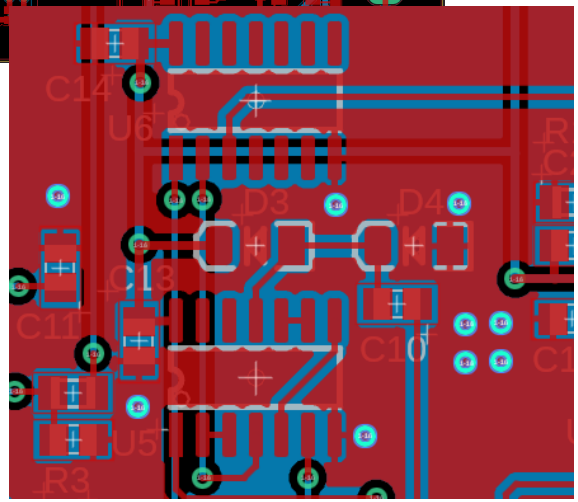
WSOS section as per TD	Points	Descriptor	Resource
3	3	• Traces are routed as short as possible. • All corners are rounded or angled by 45° (L > W). • There are meandering of all appropriate traces by requirements. • All differential signals use "Differential Pair" routing, such as USB, 485, SPI, etc. • Crystal oscillator capacitors are placed in the right place (near IC, oscillator pin, etc.) • All GND vias near the component GND pad, use multiple vias if necessary. • No other problems.	 See next page.

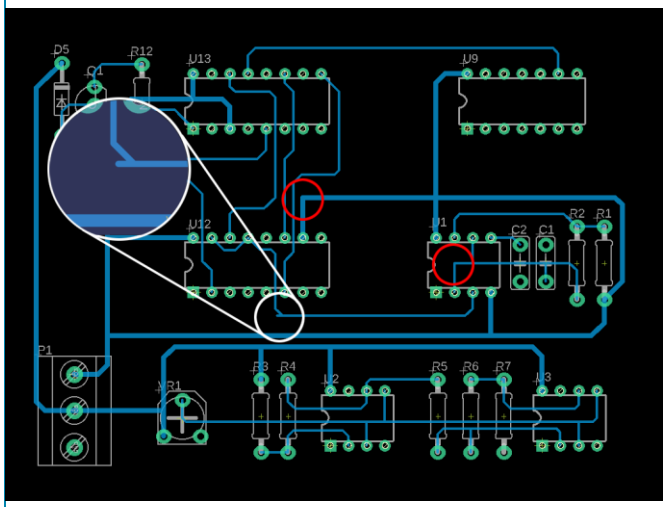
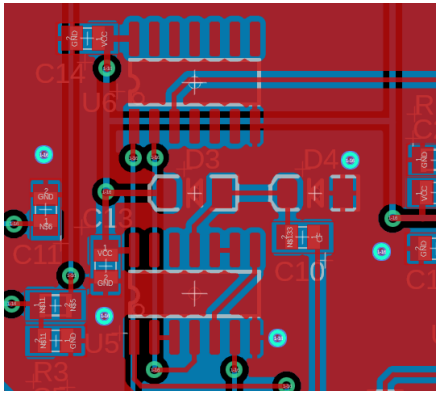
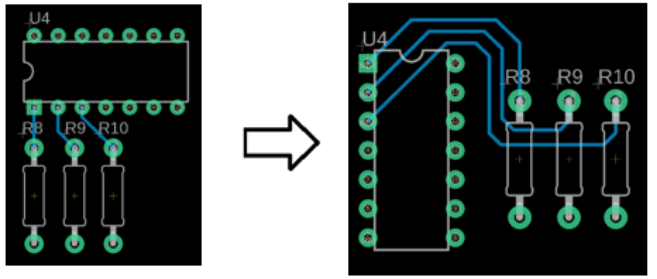

W
L
L > W

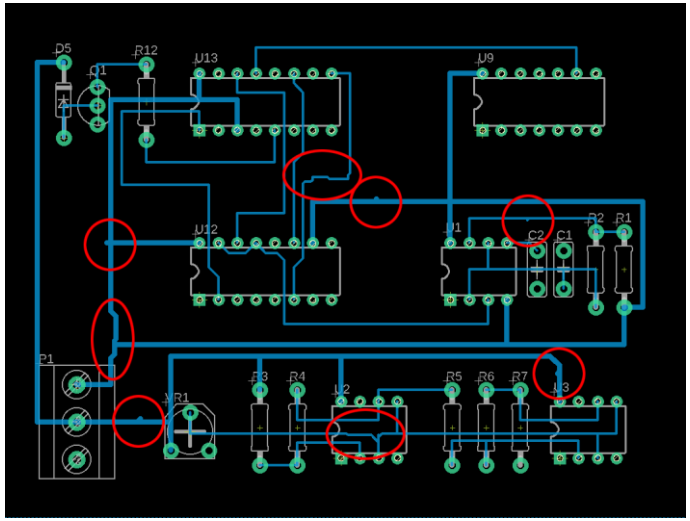
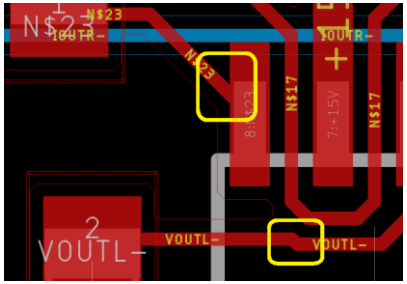
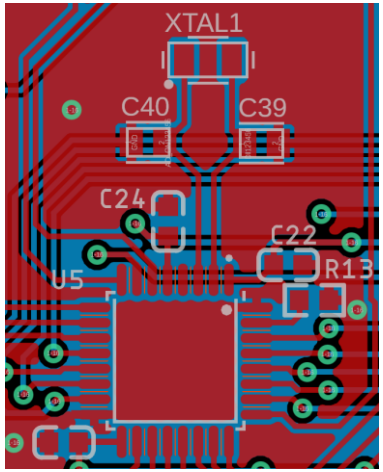
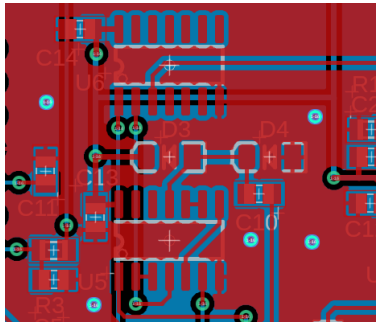
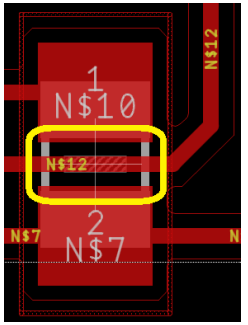


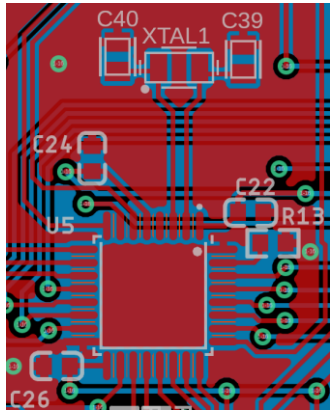
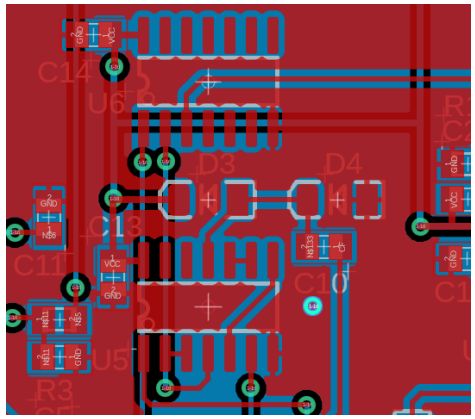
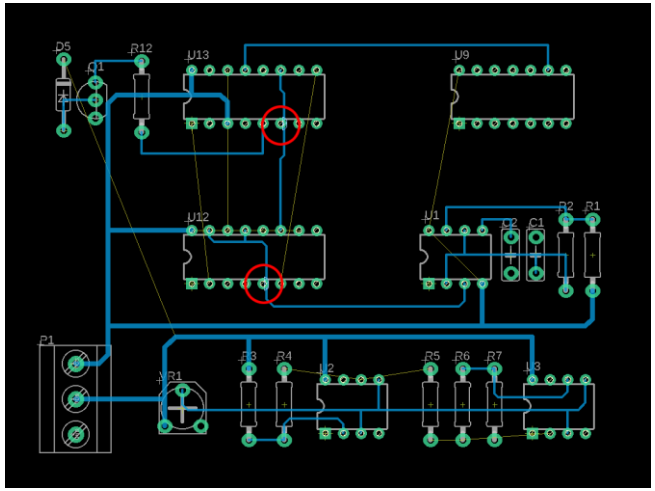
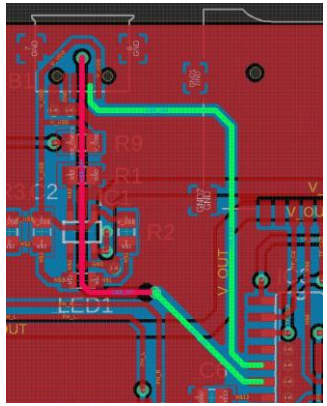

LED1


XTAL1
R16
C40
C39
C24
C22
R13
U5
C26

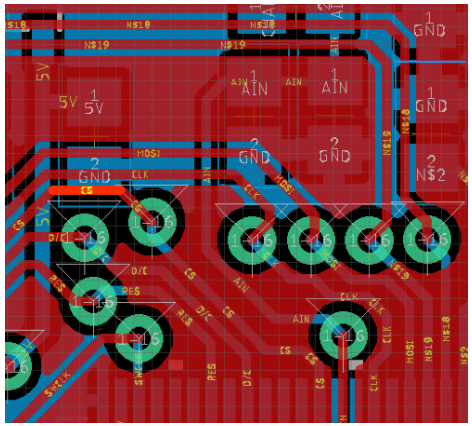
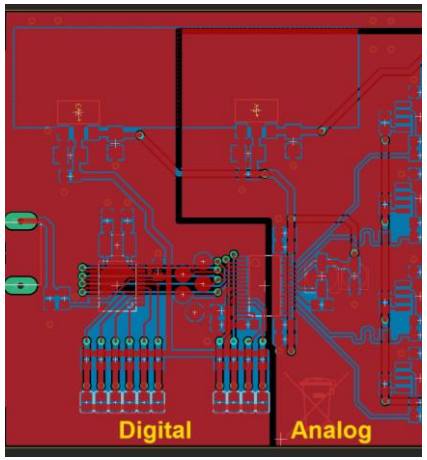
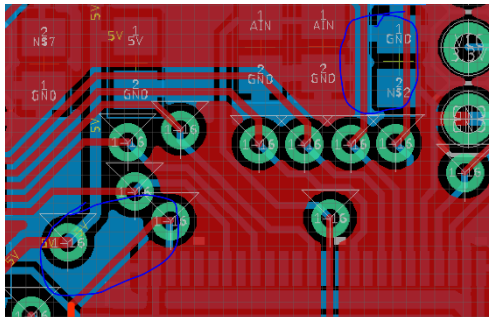


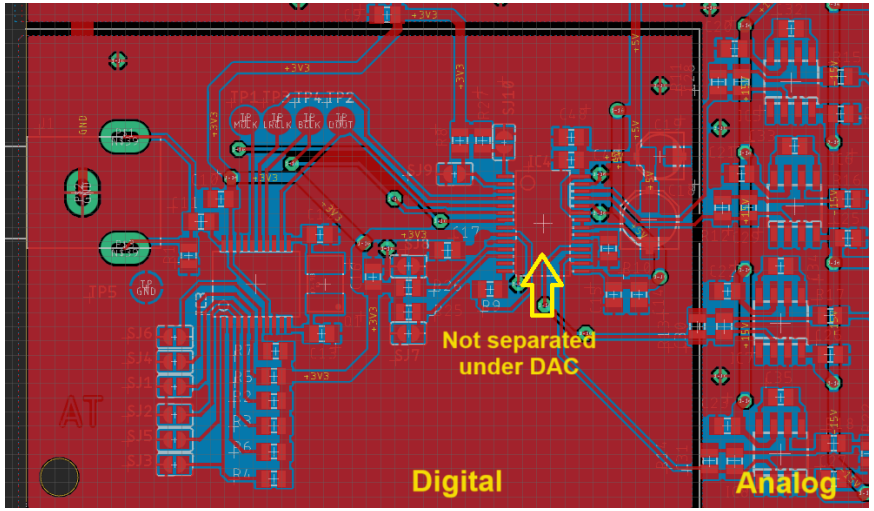
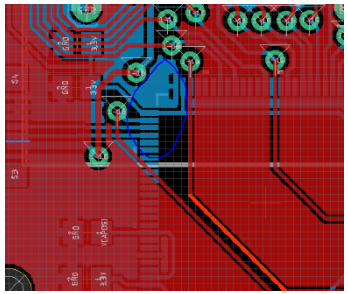
WSOS section as per TD	Points	Descriptor	Resource
3	2	• Traces are routed a bit too long. • Some corners are sharp angled. • There are some net antennae. • There are some not meandering of appropriate traces by requirements. • All differential signals use "Differential Pair" routing, such as USB, 485, SPI, etc. • Crystal oscillator capacitors are placed in the right place (near IC, oscillator pin, etc.) • All GND vias near the component GND pad, Not using multiple Vias when needed.	  

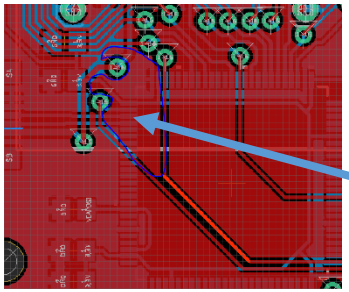
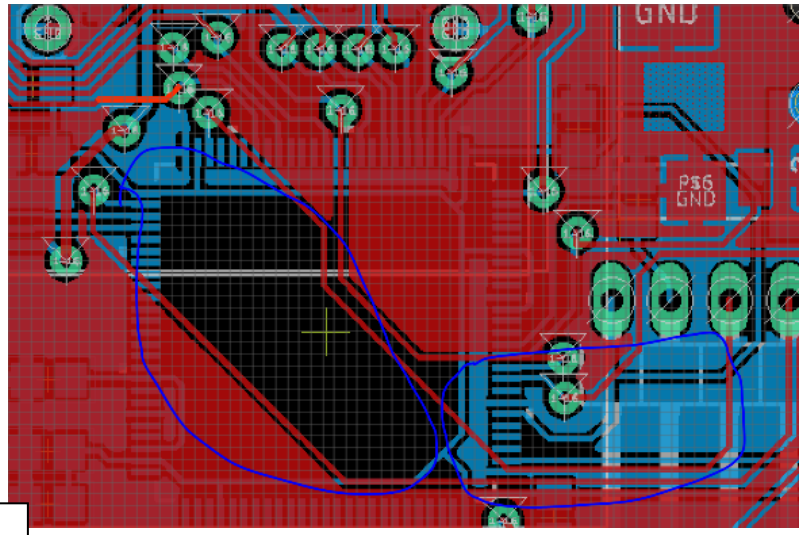
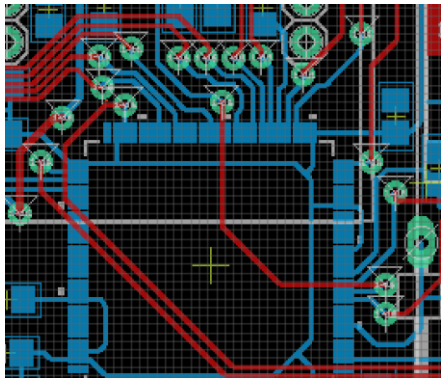
WSOS section as per TD	Points	Descriptor	Resource
3	1	• A lot of unnecessary curves. • Most corners are sharp angled. • There are many net antennae. • There is nearly no meandering of all appropriate traces by requirements. • Some traces are connected with a sharp angle to a pad. • Some traces are routed in between SMT resistor / capacitor pads. • All differential signals use "Differential Pair" routing, such as USB, 485, SPI, etc. • Crystal oscillator capacitors are placed too far from IC or oscillator pin. • Some GND vias are too far from the component GND pad, Not using multiple Vias when needed	    

WSOS section as per TD	Points	Descriptor	Resource
3	0	• Not all traces routed. • Trace overlaps with trace or hole or VIA. • There is no meandering of all appropriate traces by requirements. • Lots of traces are connected with a sharp angle to a pad. • Lots of traces are routed in between SMT resistor / capacitor pads. • The differential signals not use "Differential Pair" routing, such as USB, 485, SPI, etc. • Crystal oscillator capacitors are placed in the wrong place. • Some GND vias are missing.  	 

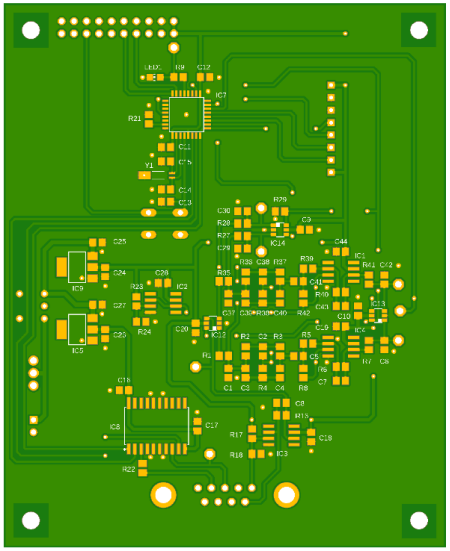
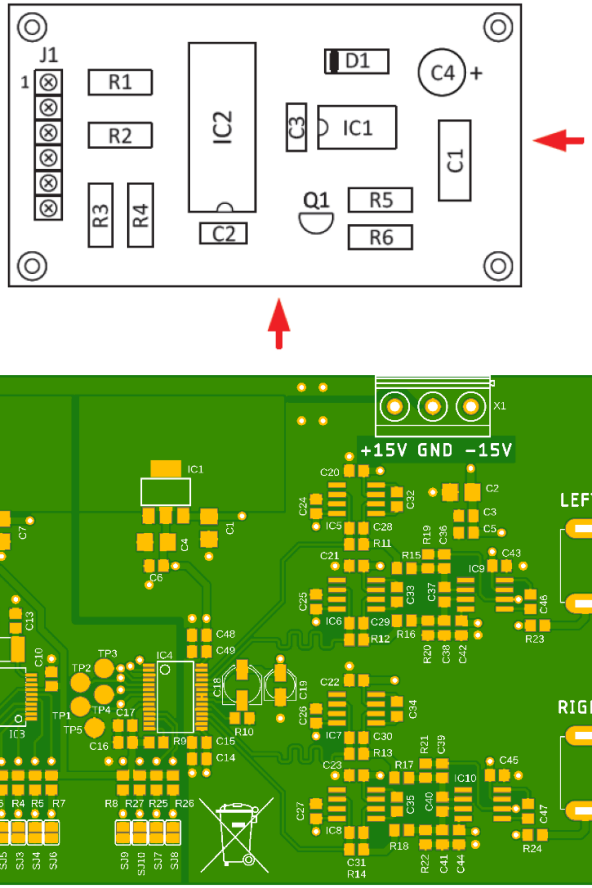
Judgement Aspect: PCB Design - Polygon Routing

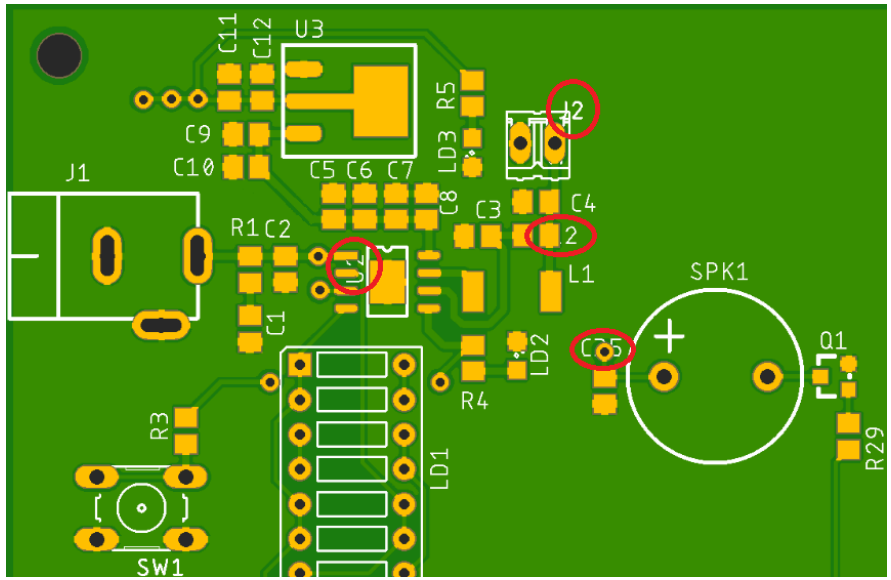
WSOS section as per TD	Points	Descriptor	Resource
1, 3	3	• No empty spaces without polygons. • All polygon sections are connected to the appropriate nets (e.g. GND). • Polygon according to instruction (e.g. analog / digital splitting, dimension requirements, etc.).	 
1, 3	2	• Some little empty spaces without polygons. • All polygon sections are connected to the appropriate nets (e.g. GND). • Polygon according to instruction (e.g. analog / digital splitting, dimension requirements, etc.).	

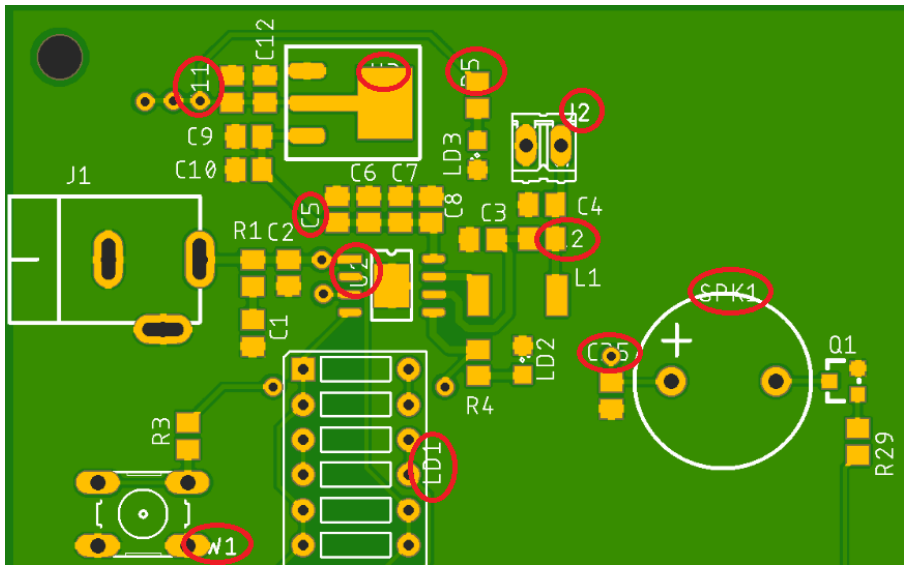
WSOS section as per TD	Points	Descriptor	Resource
1, 3	1	• Many empty spaces without polygons. • All polygon sections are connected to the appropriate nets (e.g. GND). • Polygon somewhat according to instruction (e.g. analog / digital splitting, dimension requirements, etc.).	 

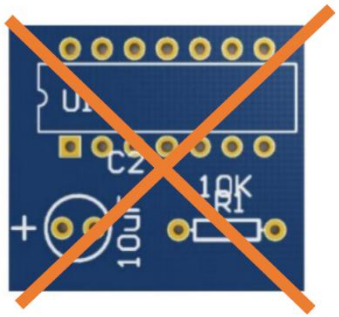
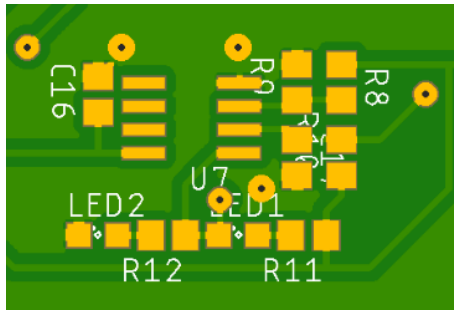
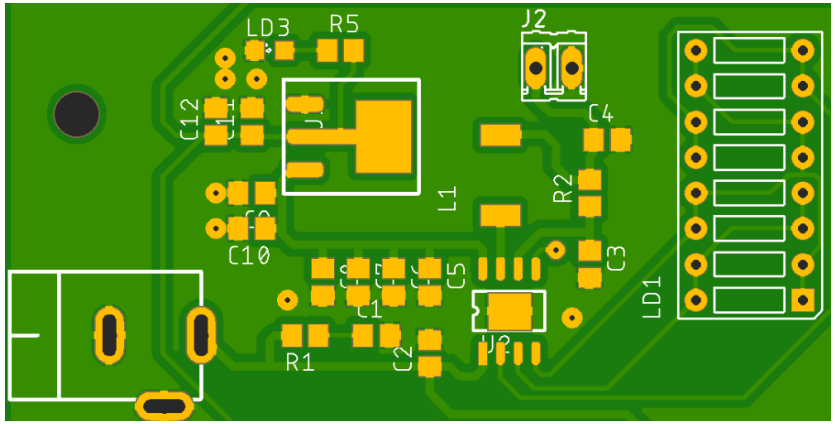
1, 3	0	• No polygons at all. • Most of the PCB area has empty spaces. • Polygon sections are not connected to the appropriate nets (e.g. GND) → orphans.  Polygon not connected	 

Judgement Aspect: PCB Design - Orientation and Placement of Component Names / Silkscreen Quality

WSOS section as per TD	Points	Descriptor	Resource
3	3	• Component names are visible and can be assigned to the corresponding component. • Text font is suitable large. • Text is readable only in two directions. • No overlap of text onto other text, outlines, vias, pads or holes. • Component values are turned off. 	

WSOS section as per TD	Points	Descriptor	Resource
3	2	• Component names are mostly visible and can mostly be assigned to the corresponding component. • Text font is suitable large. • Text is readable only in two directions. • Mostly no overlap of text onto other text, outlines, vias, pads or holes. • Component values are turned off.	

WSOS section as per TD	Points	Descriptor	Resource
3	1	• Only some component names are visible and can hardly be assigned to the corresponding component. • Text font is suitable large. • Text is readable only in two directions. • Many overlaps of text onto other text, outlines, vias, pads or holes. • Component values are turned off.	

WSOS section as per TD	Points	Descriptor	Resource
3	0	• Nearly no component names are visible and can be assigned to the corresponding component. • Text font is too small. • Text is readable in more than two directions. • A lot of overlaps of text onto other text, outlines, vias, pads or holes. • Component values are turned on. • Missing names. • No attention is paid to the silk screen at all.	  

Example Measurement Aspects: PCB Design

The following measurements are individual for every new HWD test project. Hence, they can be in there or not or some other measurements are added (e.g. separation of analog and digital GND). Also, the weighting of points is up to the Test project designer! This makes the marking form less predictable and this is what we want. The following measurements are just possible examples and are not related to the actual project:

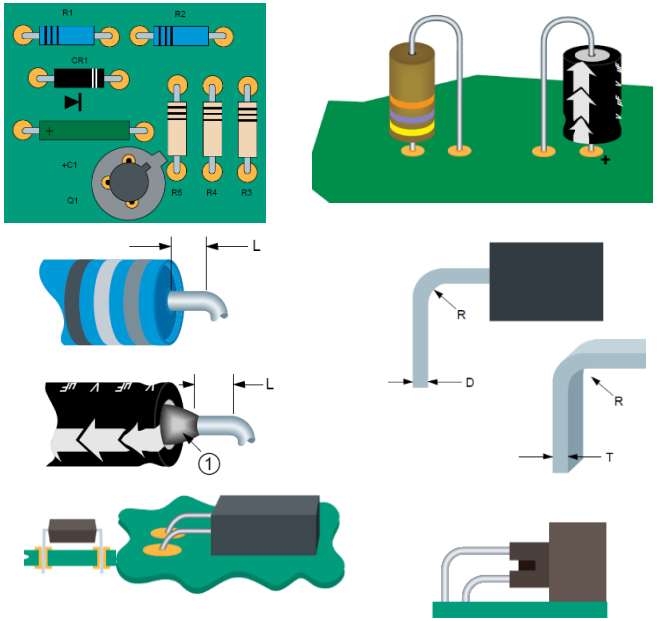
Aspect	WSOS section as per TD	Descriptor
PCB Design	3	Component library Deduct points for errors: Symbol, Footprint, Pinout errors, Dimension errors, Missing prefix, Wrong layer used, etc.
PCB Design	3	PCB dimension and shape or PCB fits into given case
PCB Design	3	Design Rule Check (DRC): Minimum clearance, Minimum trace width, Via holes correct, etc.
PCB Design	3	Minimum track width - Signals Track width for Power traces should be a judgement due to some thinner traces from bypass capacitor to IC or enable signals.
PCB Design	3	Support holes: correct placement, drill size, etc.
PCB Design	3	Components that must be placed on certain x/y/z-coordinates and angles.
PCB Design	3	DRC Errors handled / approved.
PCB Design	3	All the tracks have been routed
PCB Design	3	GND polygon - top / bottom layer
PCB Design	3	Thermal relief

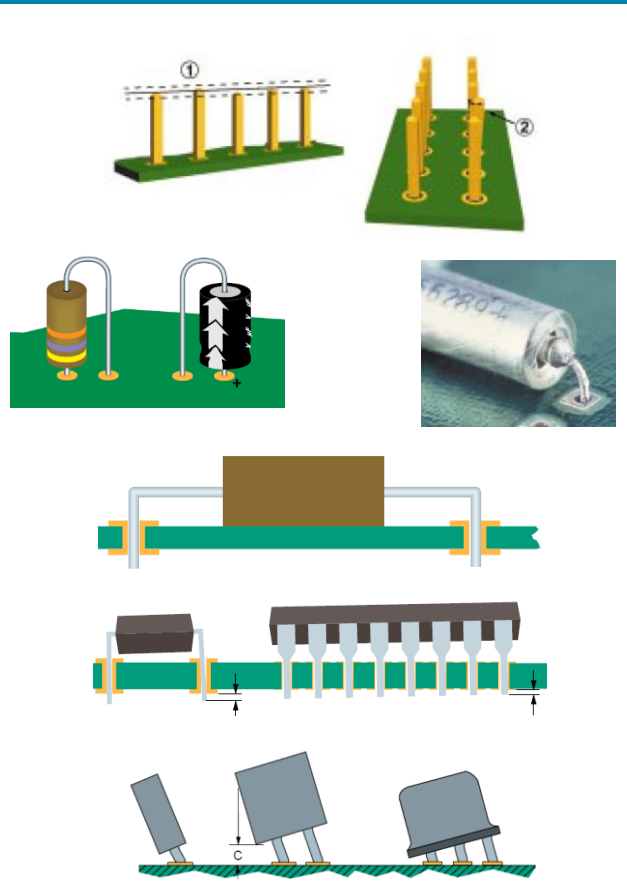
Aspect	WSOS section as per TD	Descriptor
PCB Design	3	Two letter country code on a specific layer
PCB Design	3	Gerbers, NC Drill files and BOM exported correctly
PCB Design	3	Other measurements individual for HWD test project (e.g. separation of analog and digital GND, Maximum amount of Vias, Specific polygon cutouts around holes or components etc.)
PCB Design	3	Competitor does NOT order Reference Design (own design will also be produced if producible);

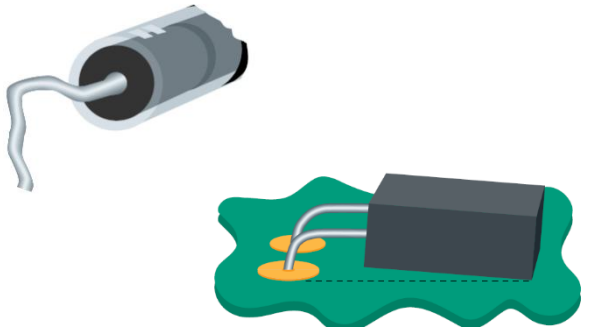
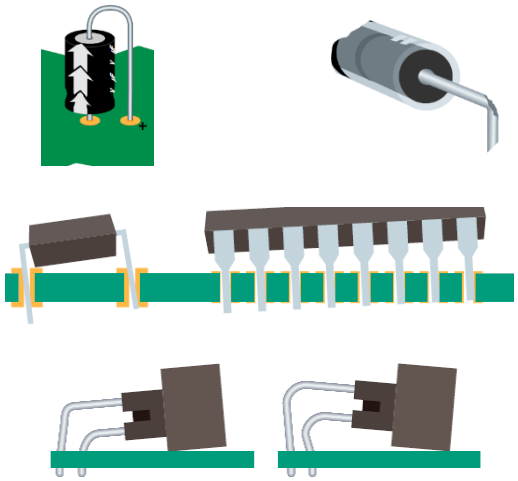
Assembly and Testing

Judgement Aspect: Assembly and Testing - THT Component Placement

Excluding VIAs

WSOS section as per TD	Points	Descriptor	Resource
4	3	• Respects IPC-A-610H Class 3 • Connector pins are straight, not twisted and properly seated. No visible damage. • Components are centred between pads, markings are visible, non-polarized components are oriented so that all read the same way (left to right or top to bottom). • Polarized part is mounted with a long ground lead. Non-polarized parts read from top to bottom. • Leads bent with minimum 1 diameter bend radius. • All leads rest on standoff step for SIPs and DIPs. • Component is perpendicular and base is parallel to board. • Component body is flat if designed to be in contact with board. • Connector sits flush to board. • All THT components are assembled.	

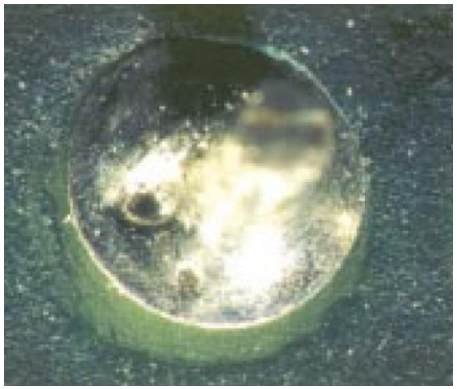
WSOS section as per TD	Points	Descriptor	Resource
4	2	• Pins are slightly off by 50% pin thickness or less. Pin height varies no more than shown. • Components are centred between pads, markings are visible, non-polarized components are not oriented so that all read the same way (left to right or top to bottom). • Polarized part is mounted with a long ground lead. Non-polarized parts read from bottom to top. • Lead bend radius is not 1 diameter or Lead bend begins too early (<0.8mm). • SIP or SIP tilted but lead protrude at a minimum length as shown. • Component tilt causes space between component base and board to be between 0.3mm and 2.0mm. • More than around 75% of THT components are assembled.	

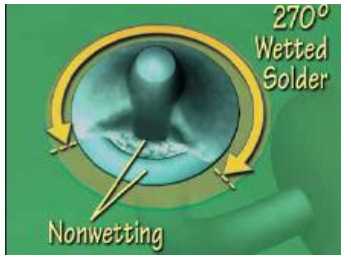
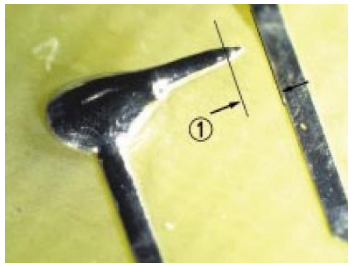
WSOS section as per TD	Points	Descriptor	Resource
4	1	• Lead is damaged between 10% and 50% of the lead diameter or length. • Component body is not 100% in contact with the board if designed to be in contact with board. • Some components have wrong and / or wrong polarized placement (e.g. electrolytic capacitor, diodes, ICs, etc.). • More than around 50% of THT components are assembled.	
4	0	• Polarized components are mounted backwards. • Lead is damaged by more than 50% of the lead diameter. • Tilt of SIP or DIP does not allow lead protrusion. • Connectors do not sit flush on board. • Lots of components have wrong and / or wrong polarized placement (e.g. electrolytic capacitor, diodes, ICs, etc.). • Less than around 50% of THT components are assembled.	

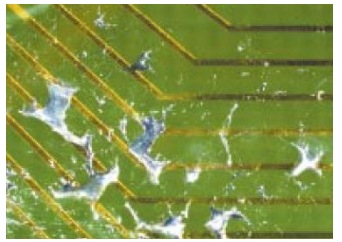
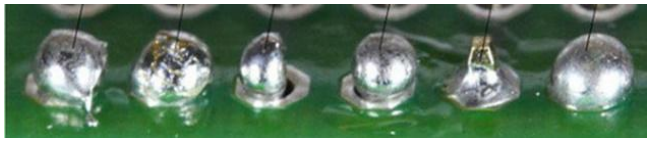
Judgement Aspect: Assembly and Testing - THT Soldering Quality

Including VIAs

WSOS section as per TD	Points	Descriptor	Resource
4	3	• Respects IPC-A-610D Class 3 • Solder fillet appears generally smooth and exhibits good wetting of the solder to the party being joined. • Outline of the parts is easily determined. • Solder at the part being joined creates a feathered edge. • Fillet is concave in shape. • Coverage is 100% of pad. • No solder splashes, no shorts. • All THT components are assembled.	  

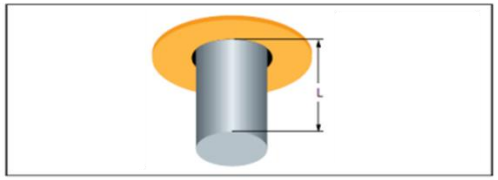
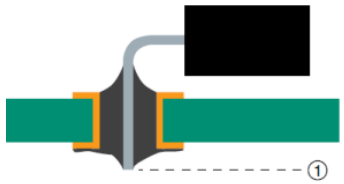
WSOS section as per TD	Points	Descriptor	Resource
4	2	• Some blow holes, pin hole visible. • Some coverage of 75 – 100% of pad. • Some small solder splashes evident but no shorts. • More than around 75% of THT components are assembled.	 

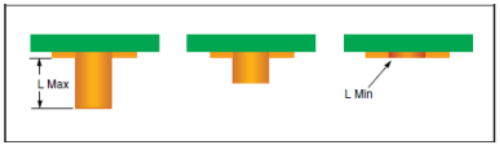
WSOS section as per TD	Points	Descriptor	Resource
4	1	• Many pads with coverage of 50% - 75% of pad. • Many solder splashes evident but no shorts. • Some poor wetting of joints. • More than around 50% of THT components are assembled.	  

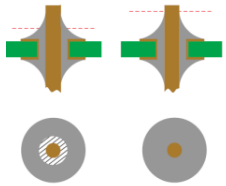
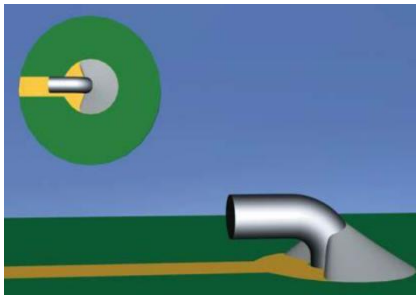
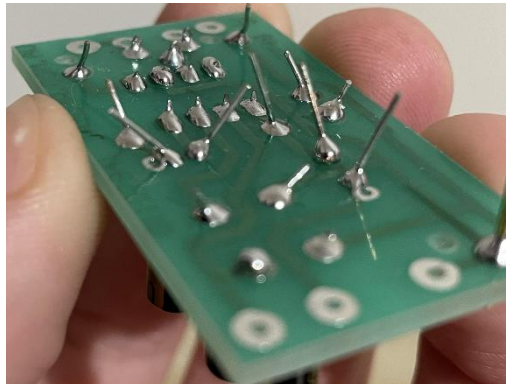
WSOS section as per TD	Points	Descriptor	Resource
4	0	• Many solder fillets do not appear smooth, good wetting of solder to the lead is not evident. • Many joints have less than 50% pad coverage. • Solder splashes evident and shorting visible. • Cold joints present. • Insufficient wetting. • Too much solder. • Less than around 50% of THT components are assembled.	     

Judgement Aspect: Assembly and Testing - THT Leads - Quality of leads (cutting, bending, ...)

Including VIAs

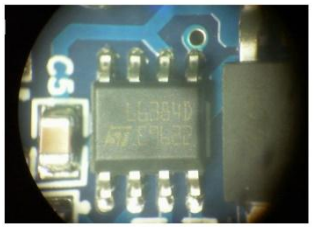
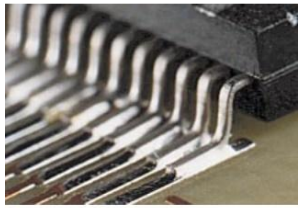
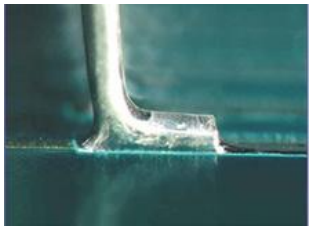
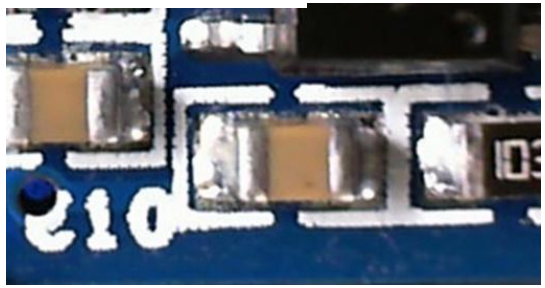
WSOS section as per TD	Points	Descriptor	Resource
4	3	• Respects IPC-A-610D Class 3 • Almost all leads are cut perfectly. • Almost all cut leads are straight. • All THT components are assembled.	 **Acceptable - Class 1,2,3** • The leads protrude beyond the land within the specified minimum and maximum (L) of Table 7-3, provided there is no danger of violating minimum electrical clearance. • The leads meet the design length (L) requirements when specified. **Table 7-3 Protrusion of Wires/Leads in Supported Holes** Class 1 / Class 2 / Class 3 (L) min. — End is discernible in the solder.[1] (L) max.[2] — No danger of shorts / 2.5 mm [0.0984 in] / 1.5 mm [0.059 in] **Note 1.** For components having manufacturer's pre-established lead lengths that are less than board thickness, and the components or lead shoulders are flush to the board surface, the lead end is not required to be visible in the subsequent solder connection, see 1.4.1.5. **Note 2:** Connector leads, relay leads, tempered leads and leads greater than 1.3 mm [0.050 in] diameter are exempt from the maximum length requirement provided that they do not violate minimum electrical spacing.  Acceptable – Class 1, 2, 3 No fractures between lead and solder Lead protrusion with in specification

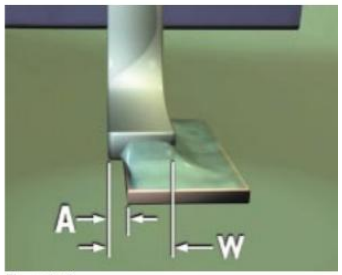
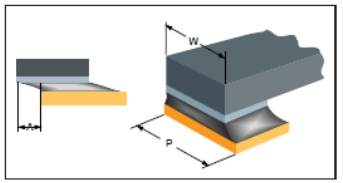
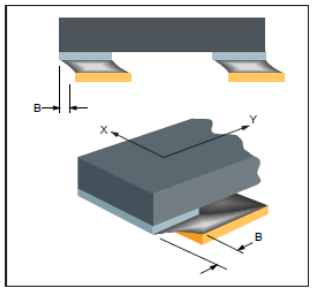
WSOS section as per TD	Points	Descriptor	Resource
4	2	• Almost all leads are cut acceptably. • Almost all cut leads are straight. • More than around 75% of THT components are assembled.	 **Figure 7-77** **Defect - Class 1,2,3** • Lead protrusion does not meet the requirements of Table 7-3. • Lead protrusion violates minimum electrical clearance. • Lead protrusion exceeds maximum design height requirements. **Table 7-3 Protrusion of Wires/Leads in Supported Holes** | | Class 1 | Class 2 | Class 3 | | (L) min. | End is discernible in the solder.[1] | | | | (L) max.[2] | No danger of shorts | 2.5 mm [0.0984 in] | 1.5 mm [0.059 in] | **Note 1.** For components having manufacturer's pre-established lead lengths that are less than board thickness, and the components or lead shoulders are flush to the board surface, the lead end is not required to be visible in the subsequent solder connection, see 1.4.1.5. **Note 2:** Connector leads, relay leads, tempered leads and leads greater than 1.3 mm [0.050 in] diameter are exempt from the maximum length requirement

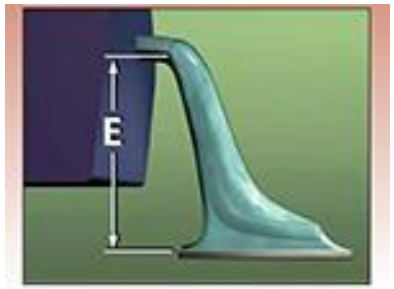
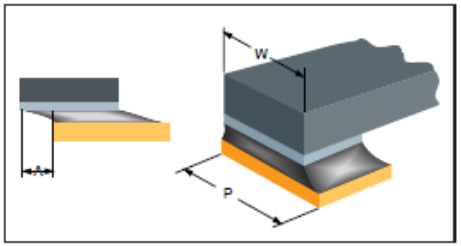
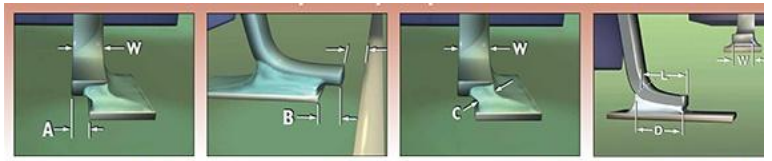
WSOS section as per TD	Points	Descriptor	Resource
4	1	• Some leads are cut acceptably, but also cut into solder fillet. • Many cut leads are bend. • More than around 50% of THT components are assembled.	 Defect – Class 1, 2, 3 Evidence of fracture between lead and solder fillet Defect – Class 3 Lead trimming that cuts into the solder fillet and is not reflowed
4	0	• Too many leads are too long and could cause short circuits. • Too many leads are cut into solder joint. • Too many cut leads are bend. • Less than around 50% of THT components are assembled.	 

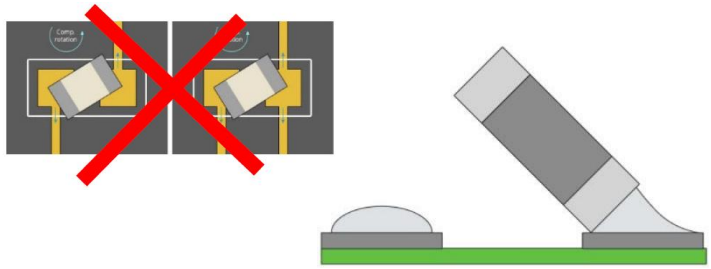
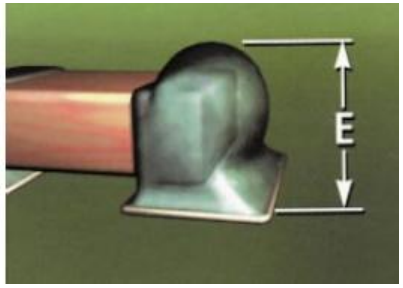
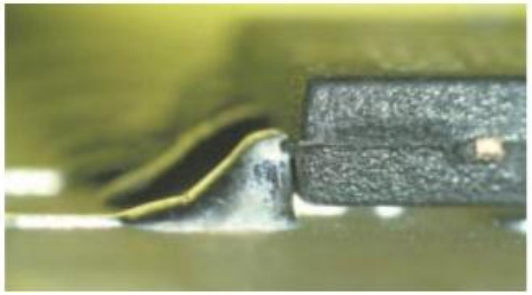
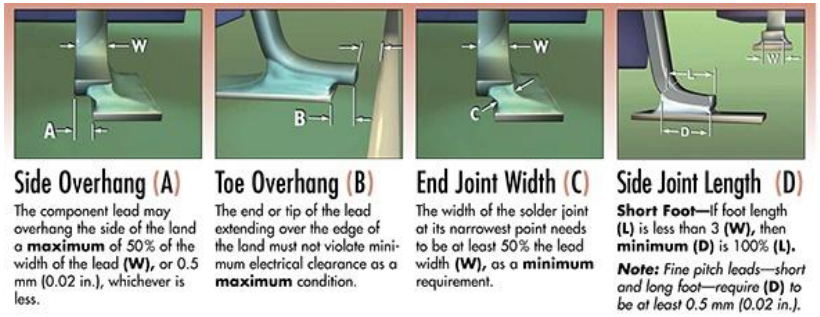
Judgement Aspect: Assembly and Testing - SMT Component Placement and Soldering

Separated into two judgements in marking form: **SMT Soldering Quality** and **SMT Component Placement**

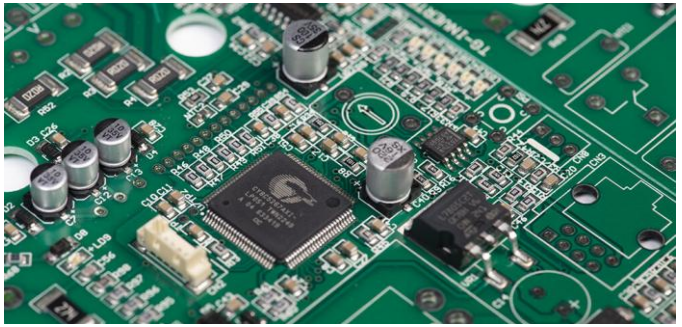
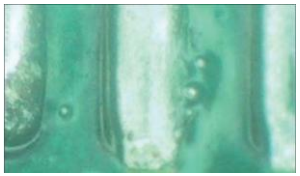
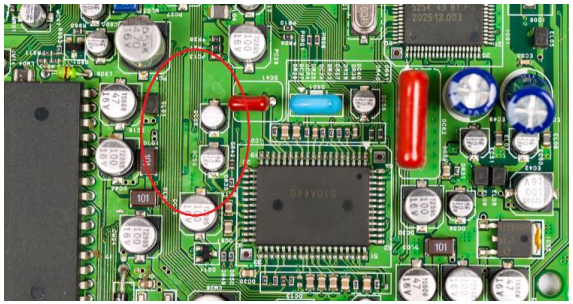
WSOS D	Points	Descriptor	Resource
4	3	Respects IPC-A-610D Class 3 **Component Placement:** • Component centred on pads side to side and front to back. **Soldering:** • Solder fillet appears generally smooth and exhibits good wetting of the solder to the party being joined. • Ideal amount of solder on leads. • No solder splashes, no shorts. • All SMT components are assembled.	  Figure 8-81   Figure 8-82 

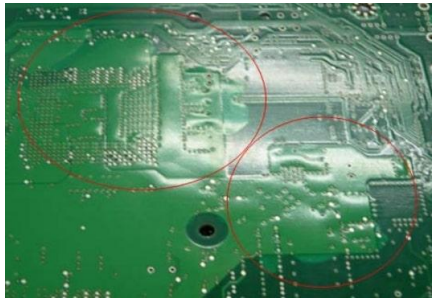
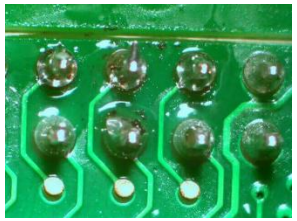
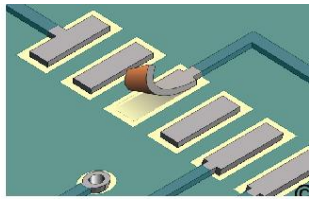
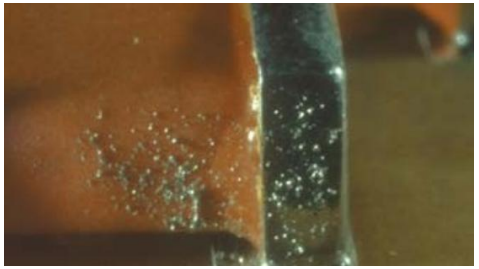
WSOS section as per TD	Points	Descriptor	Resource
4	2	**Component Placement:** • Some slight misalignments on pads front to back or side to side. -Maximum overhang (A) is not greater than 25% lead width (W) or 0.5mm [0.02in], whichever is less. • Slight misalignment on pads front to back or side to side. Side overhang (A) is less than 25% of the width (W) or 25% width of land (P). • No end overhang evident. **Soldering:** • Some small solder splashes evident but no shorts. • More than around 75% of SMT components are assembled.	  Figure 8-71  Figure 8-5  Figure 8-6

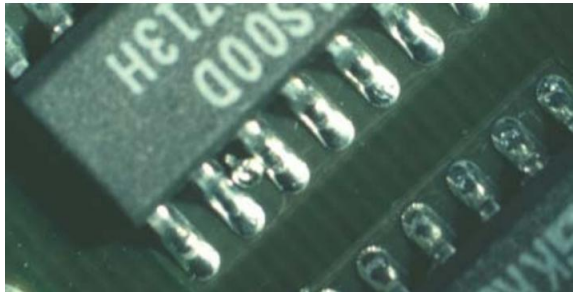
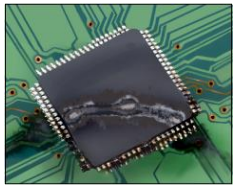
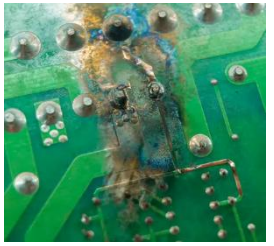
WSOS section as per TD	Points	Descriptor	Resource
4	1	**Component Placement:** • Some significant misalignments on pads front to back or side to side. Side overhang (A) is less than 50% of the width (W) or 50% width of land (P). • Some components have wrong and / or wrong polarized placement (e.g. electrolytic capacitor, diodes, ICs, etc.). **Soldering:** • Excessive solder but not touching other components or leads and "balling" not evident. • Some Poor wetting of joints. • Many Solder splashes evident but no shorts. • More than around 50% of SMT components are assembled.	  Figure 8-74  Figure 8-5  **Side Overhang (A)** The component lead may overhang the side of the land a **maximum** of 50% of the width of the lead **(W),** or 0.5 mm (0.02 in.), whichever is less. **Toe Overhang (B)** The end or tip of the lead extending over the edge of the land must not violate minimum electrical clearance as a **maximum** condition. **End Joint Width (C)** The width of the solder joint at its narrowest point needs to be at least 50% the lead width **(W),** as a **minimum** requirement. **Side Joint Length (D** **Short Foot—**If foot length **(L)** is less than 3 **(W),** then **minimum (D)** is 100% **(L).** ***Note:** Fine pitch leads—sha and long foot—require* **(D)** *be at least 0.5 mm (0.02 in.,*

WSOS section as per TD	Points	Descriptor	Resource
4	0	**Component Placement:** • Some huge misalignments on pads front to back or side to side. • Lots of components have wrong and / or wrong polarized placement (e.g. electrolytic capacitor, diodes, ICs, etc.). • End overhang evident. • Tombstoning evident. **Soldering:** • Excessive soldering, "balling" evident. • Solder touching body. • Solder touching other components or leads. • Solder splashes evident and shorting visible. • Cold joints present. • Insufficient wetting. • Too much solder. • Less than around 50% of SMT components are assembled. 	  Figure 8-74  

Judgement Aspect: Assembly and Testing - PCB damage & component damage & flux residues

WSOS section as per TD	Points	Descriptor	Resource
4	3	• No noticeable flux residues. • No noticeable PCB or component damage. • No visible solder balls.	
4	2	• Some areas show excess heat applied. • Light pollution, flux residues largely removed. • Almost no PCB or component damage. • A small amount of solder balls appeared in some areas 	 

WSOS section as per TD	Points	Descriptor	Resource
4	1	• Medium pollution, flux residues slightly removed. • Nearly no PCB or component damage. • Some pads have lifted but are still connected. • Many amount of solder balls appeared in some areas 	  *Lifted Pad in a Through-Hole PCB*  *Lifted Pad in a Surface Mount PCB* 

WSOS section as per TD	Points	Descriptor	Resource
4	0	• PCB is very dirty. • Flux residues are not removed at all. • PCB or components are noticeable damaged. • There are too many damaged pads or overheated areas. • There are too many amount of solder balls appeared in some areas, and there is a situation that causes a short circuit 	     

Example Measurement Aspects: Assembly

Aspect	WSOS section as per TD	Descriptor
Assembly	4	No repaired / added connections → PCB without modification. E.g. added wires for missing or wrong traces, open nets, airwires
Assembly	4	All vias soldered.
Assembly	4	All components soldered / assembled. Only check whether all components are placed, polarity does not matter here. Polarity will be assessed in Placement Judgements

Example Measurement Aspects: Testing

Aspect	WSOS section as per TD	Descriptor
Testing / Measurement	7	Functionality X Oscilloscope screen capture X shows the voltage value (<1V) (+/- 10%) at pin DC.
Testing / Measurement	7	Functionality X Oscilloscope screen capture X shows the PWM signal with an amplitude of 3.3V (+/- 10%), a frequency of 1kHz (+/- 10%) and a duty cycle of 50% (+/- 10%) at pin PWM1.
Testing / Measurement	7	Functionality X Oscilloscope screen capture X shows a gain of the amplifier of 10 (+/- 5%) at pin AMP.
Testing / Measurement	7	Functionality X Oscilloscope screen capture X shows a triangular signal with an amplitude of 5V (+/- 5%) and a frequency of 1MHz (+/- 10%) at pin TRI.
Testing / Measurement	4	PCB can be powered on without short circuit.
Testing / Measurement	4	The LEDs (LED20 and LED21) at the corresponding positions of the solar panel connector (V-SUN) and battery connector(V-BAT) can light up normally, and the colour of the LEDs will change according to the voltage of the Port.

Testing is measurements only, individual for every new Assembly and Testing test project. The measurements are up to the test project designer. The following measurements are just possible examples and are not related to the actual project:

Embedded Systems Programming

Possible Measurement Aspects: Embedded Systems Programming

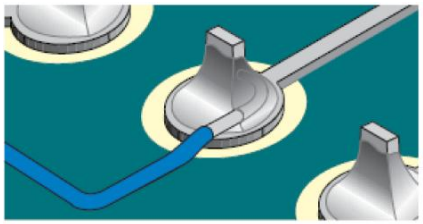
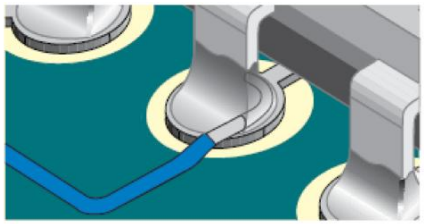
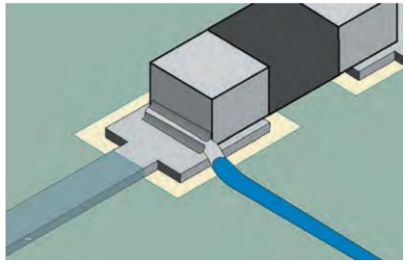
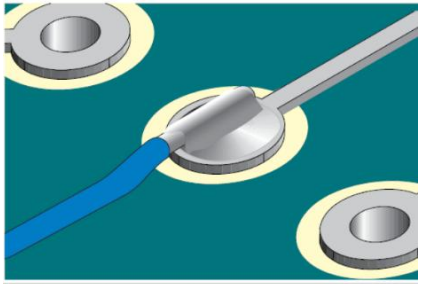
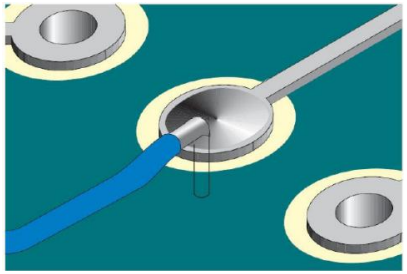
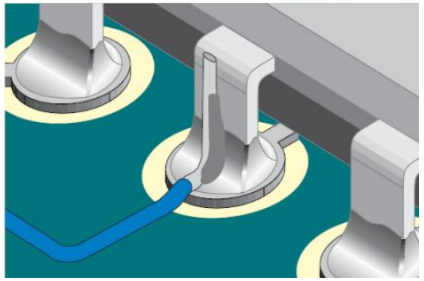
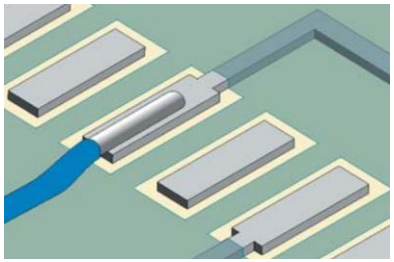
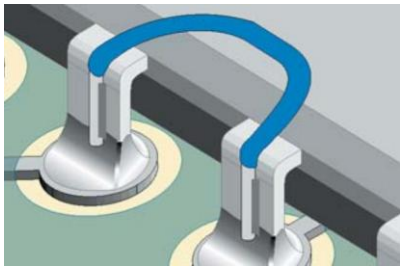
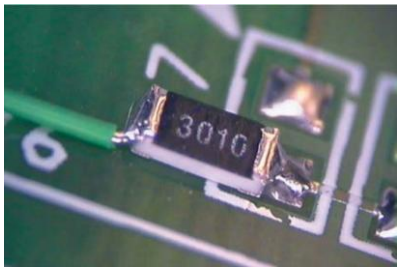
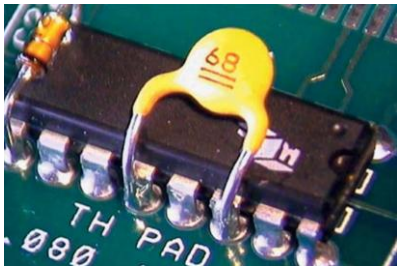
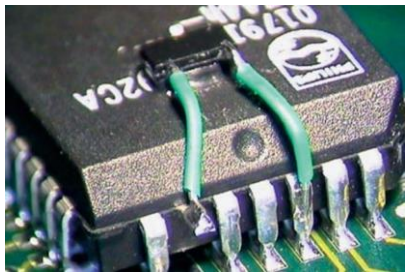
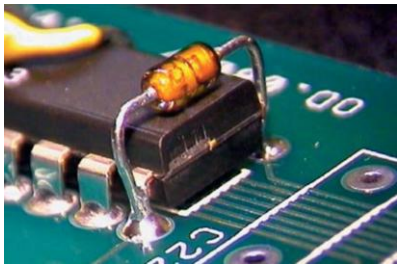
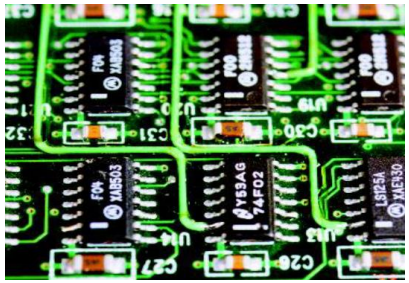
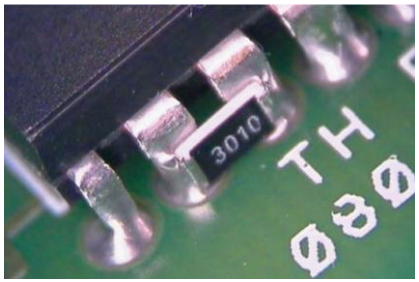
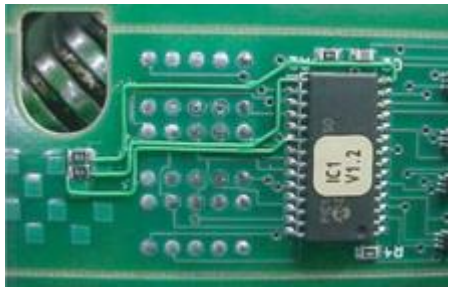
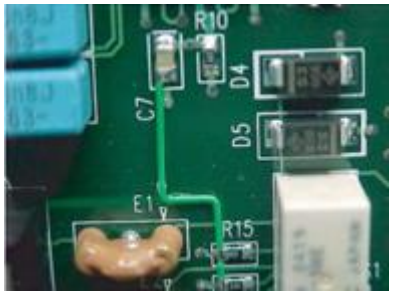
Aspect	WSOS section as per TD	Descriptor
ESP	6	Main screen or screen X: The display pattern is according to documentation
ESP	6	Control sequence of display
ESP	6	Font size, Font colour, Background colour of display are correct. Separate into multiple measurements
ESP	6	Sensor (I²C, SPI, etc.) values are read, displayed and refreshed correctly on the display. Separate into multiple measurements
ESP	6	ADC values are read, displayed and refreshed correctly on the display. Separate into multiple measurements.
ESP	6	The control software for switches, buttons, rotary encoders, etc. is implemented according to the instructions. Separate into multiple measurements.
ESP	6	USB, UART communication are working correctly. Separate into multiple measurements.
ESP	6	PWM has correct frequency and Duty Cycle
ESP	6	Certain variables / values are still available after power ON / OFF.

*** Measurements only, individual for every new Embedded Systems Programming test project. The measurements are up to the test project designer. The following measurements are just possible examples and are not related to the actual project**

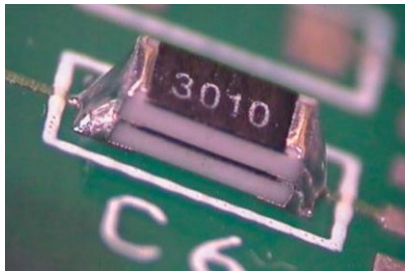
Modification Quality

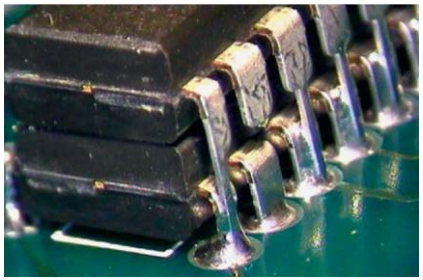
Judgement Aspect: Modification and Measurement - Modification Quality

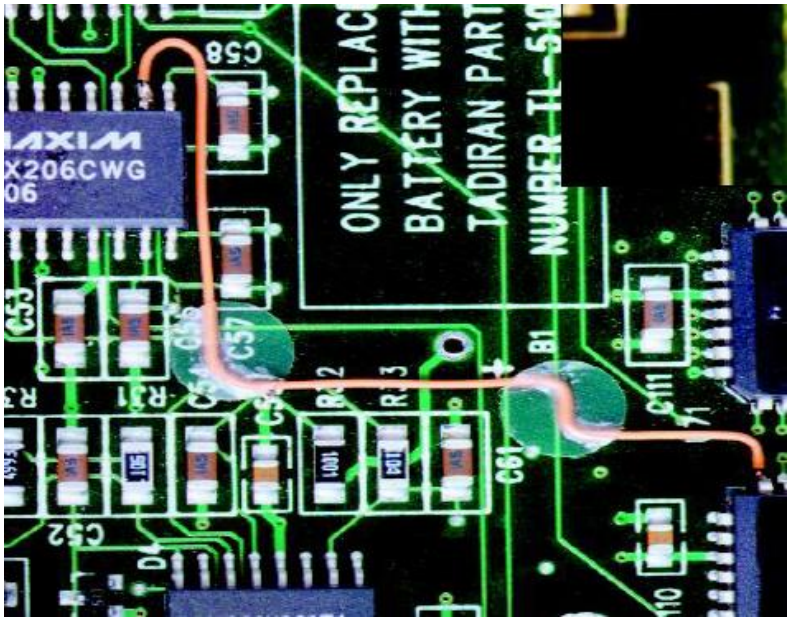
WSOS section as per TD	Points	Descriptor	Resource
5，4	3	• Modification is done according to IPC 7711A/7721A and IPC-A-610D standards Class 3 • Performance wholly exceeds industry standard and is judged as excellent Target – Class 1, 2, 3 •Wire routed shortest route. •Wire does not pass over or under components. •Wire does not pass over land patterns or vias used as test points. •Wire does not cross component footprint or lands.	• THT / SMT component placement and soldering see Assembly & Testing. See next page.

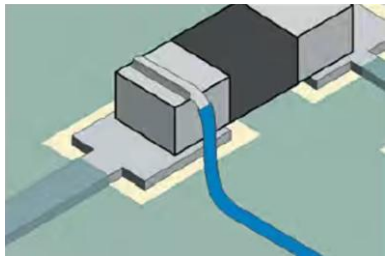









3010

TH PAD




3010
TH

IC1
V1.2

R10
D4
C7
D5
R15

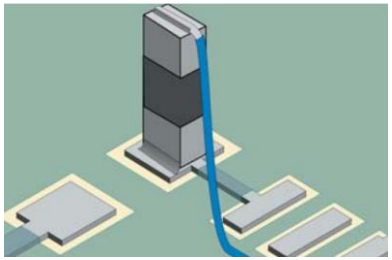
WSOS section as per TD	Points	Descriptor	Resource
5，4	2	• Modification is almost done according to IPC 7711A/7721A and IPC-A-610D standards Class 3 • Performance meets and, in specific respects, exceeds industry standard (pg 353 - 363).	• THT / SMT component placement and soldering see Assembly & Testing. *See next page.

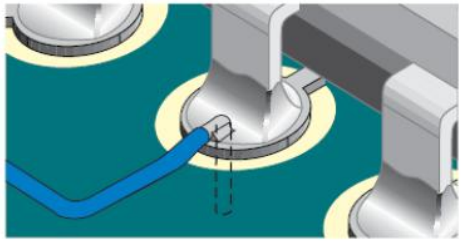


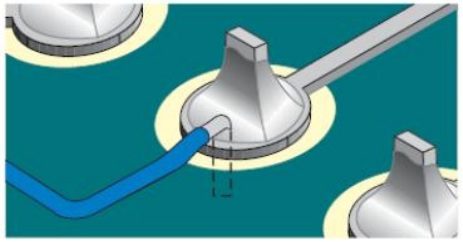






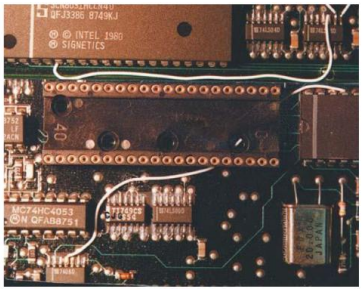
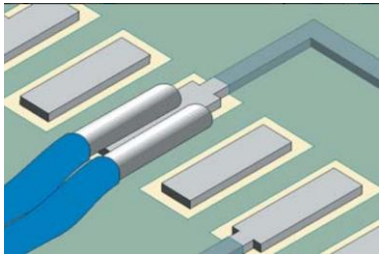
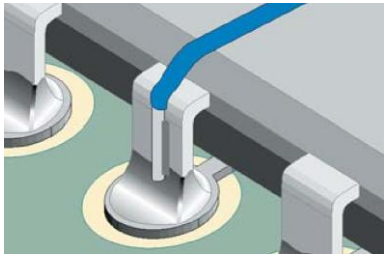


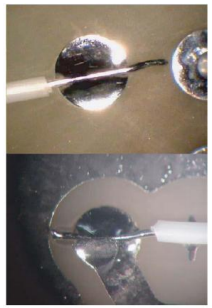
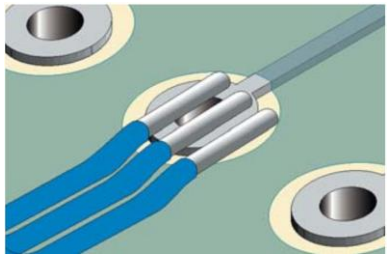
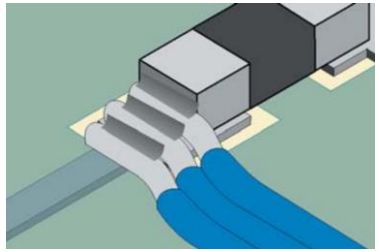
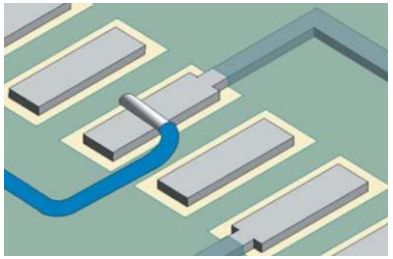
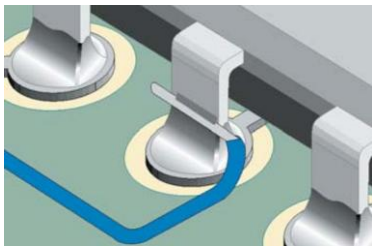




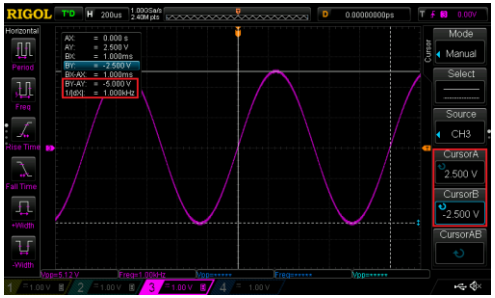
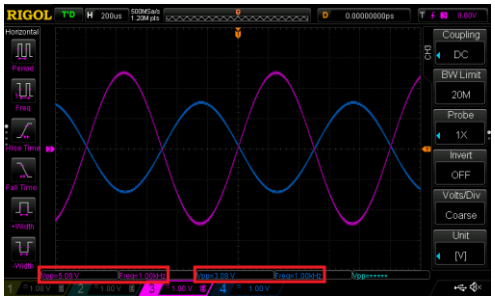
Acceptable – Class 1, 2

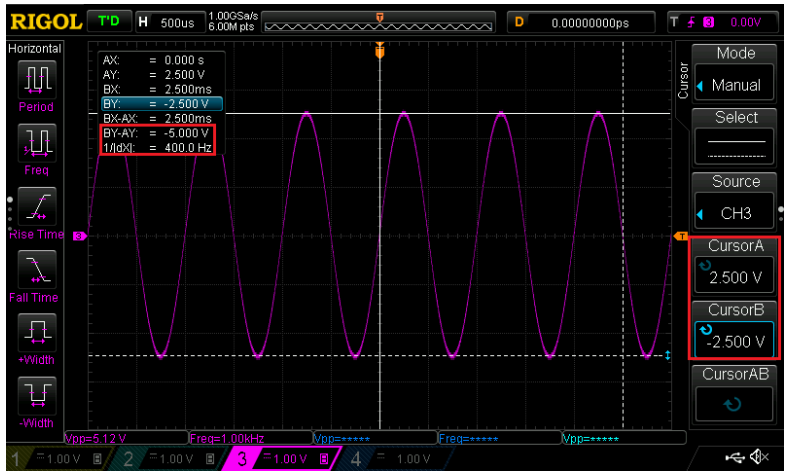
Defect – Class 3

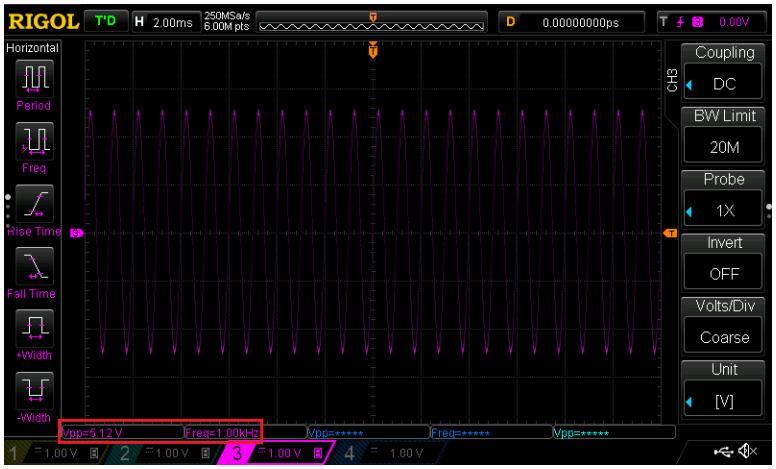
WSOS section as per TD	Points	Descriptor	Resource
5，4	1	• Modification is slightly done according to IPC 7711A/7721A and IPC-A-610D standards Class 3 • Performance meets industry standard (pg 353 - 363).	• THT / SMT component placement and soldering see Assembly & Testing.  Acceptable – Class 1 Defect – Class 2, 3 •Wire routed under or over components. •Routing of wire(s) overhang or wrap over the edge of the board.  

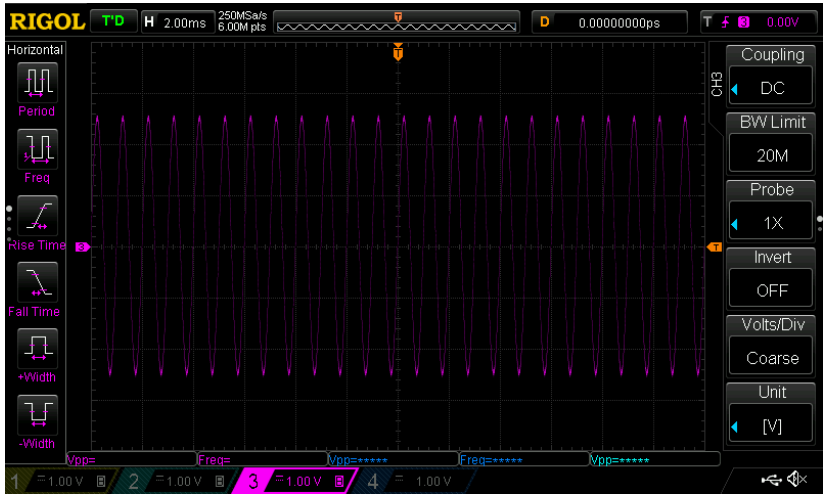
WSOS section as per TD	Points	Descriptor	Resource
5，4	0	• Modification is not done according to IPC 7711A/7721A and IPC-A-610D standards. • Performance below industry standard (pg 353 - 363). • Modification / Measurement was not performed correctly.	• THT / SMT component placement and soldering see Assembly & Testing.  Defect – Class 1, 2, 3 •Wire that is lap soldered is less than 75% from edge of land to knee of lead. •Wire extends beyond the knee of lead. •Lead violates minimum electrical clearance.    

Judgement Aspect: Modification and Measurement - Documentation / Measurement Quality

WSOS section as per TD	Points	Descriptor	Resource
7	3	• The modification description is understandable and the right symbols are used. • The measurement setup is filled out correctly. • The description and modification evidence shows clear and understandable measurements and / or correct symbols are used. • The oscilloscope measurement is perfectly understandable (see also Circuit Design - Simulation Quality - 3P)	See Recording Modification and Measurement_Instructions.pdf  

WSOS section as per TD	Points	Descriptor	Resource
7	2	• The modification description is understandable and the right symbols are mostly used. • The measurement setup is filled out almost correctly. • The description and modification evidence shows clear and understandable measurements and / or correct symbols are mostly used. • The oscilloscope measurement is well understandable (see also Circuit Design - Simulation Quality - 2P). 	See Recording Modification and Measurement_Instructions.pdf

WSOS section as per TD	Points	Descriptor	Resource
7	1	• The modification description is somehow understandable, but some wrong symbols are used. • The measurement setup is filled out almost correctly. • The description and modification evidence shows somehow understandable measurements, but some wrong symbols are used. • The oscilloscope measurement is somewhat understandable (see also Circuit Design - Simulation Quality - 1P). 	See Recording Modification and Measurement_Instructions.pdf

WSOS section as per TD	Points	Descriptor	Resource
7	0	• The modification description is not understandable and wrong symbols are used. • The measurement setup is filled out wrong. • The description and modification evidence shows not understandable measurements and wrong symbols are used. • Modification / Measurement was not performed correctly. • The oscilloscope measurement is not understandable at all (see also Circuit Design - Simulation Quality - 0P) 	See Recording Modification and Measurement_Instructions.pdf

Example Measurement Aspects: Modification and Measurement

The following measurements are just possible examples and are not related to the actual project:

Aspect	WSOS section as per TD	Descriptor
Modification and Measurement	5, 4	The component(s) for modification X have been identified and re-calculated correctly.
Modification and Measurement	5, 4	The component(s) for modification X has / have been modified correctly.
Modification and Measurement	5, 4	The component(s) for repair X has / have been done correctly.
Modification and Measurement	5, 4	X is / are measured correctly.

Skill-specific notes on assessment

- **For judgement**, a reasonable time limit for inspection of the assessment criteria must be chosen by the assessment team to allow efficient marking.
- **Circuit Design**: First, Experts do the measurements of the circuit task to be assessed in order to understand if the circuit works or not. This is relevant for judgement.
- **PCB Design**: 30 minutes after the start of the competition, all Competitors submit component footprint library files, and then SCM hand out the reference footprint files for PCB design
- **PCB Design**: Gerbers, NC Drill files and BOM exporting: If no files are submitted or not OK, 0 points are awarded and the files are exported by experts.
- **PCB Design**: If the own PCB layout is chosen but violates the design rules, the PCB will be produced with the next available tools.
- **Assembly**: The assembled PCBs must not be ranked from good to bad. Every expert should make their own opinion of the assembled PCBs.
- **Assembly**: First, assess all SMT related aspects of all PCBs. Second, assess all THT related aspects of all PCBs and so on. Do not assess all aspects of one PCB and then go to the next.
- **Testing:** If there is a criterion which should be tested by the assessment group, since no screen captures are mandatory, this should be done at the workplace of the competitor.
- Assessment of **Embedded Systems Programming - Phase 1** is done at the workplace of the Competitor during the competitor's lunch if allowed by the SMP.
- Assessment of **Embedded Systems Programming - Phase 2** is done at the workplace of the Competitor.
- **Embedded Systems Programming:** Experts need to determine the evaluation criteria before marking, such as test input conditions, number of press button, input parameters, and allowed Reset times for each Competitor’s work.